

Quicksilver_MLK Design

POWER

AC/BATT
CONNECTOR PG 57

BATT
CHARGER PG 50

CLK GEN

SLG8SP585 PG 5

SYSTEM POWER

SUS/ RUN POWER SW

+V5_SUS / +V5_RUN / +V1.5_RUN
+3.3V_ALW / +V3.3A_PCH / +V3.3_SUS / +V3.3_RUN PG 58

CPU VR
+VCC_CORE PG 51

VR
+V1.1S PG 52

VR
+V1.1S_VTT PG 53

REGULATOR For DDR3
+1.5V_DDR
+0.75V_DDR_VTT PG 54

REGULATOR
+5V_ALW
+3.3V_ALW_17020 PG 55

LDO
+V1.8S PG 56

Dual/Quad Core CPU
Intel
Arrandale / Clarksfield
(35W 2C/45W,55W 4C)
(989 rPGA)
37.5 x 37.5 mm
PG 6-12

DDR III

DDR3-SODIMM PG 14

DDR III

DDR3-SODIMM PG 15

PCIEx8

MXM CONNECTOR 2 PG 27-28

PCIEx8

MXM CONNECTOR 1 PG 25-26

HDMI

HDMI Connector PG 34

DP-A

VGA

CRT CONN PG 32

DP-D

eDP Connector PG 29

Panel Connector

LVDS

LVDS Connector PG 31

DP-C

Display Port PG 34

DMI X 4

Intel
Ibex Peak M
(1071 Pin PBGA)
27 x 25 mm
PG 16-24

USB2.0

PCI-E

USB2.0

WiMax Half
MINI-CARD PG 38

I2C

Light FX
PG 44, 45

Keyboard BL
T/P Module

Head Logo - A

Logo - B

Speaker LED

PCI-E

USB2.0

UWB/BT MINI-CARD
PG 39

PCI-E

USB2.0

RGMII

Express Card

Audio/ Express Board 3/3

Express Switch
RICOH
R5538D001
(20 QFN)
4 x 4 mm

PHY
HANKSVILLE
82577LC
(48 BGA)
6 x 6 mm PG 47

Magnetic PG 48

RJ45 PG 48

SPI

FLASH Memory
FOR SYSTEM
(8 Pin SO8W)
PG 16

LPC

SIO
ITE
ITE8512E
(128 Pin LQFP)
16 x 16 mm PG 41

SM Bus

SPI

MAX7313 X 3
PG 44

FLASH Memory
2MB
(8 Pin SO8W)
PG 42

Keyboard PG 43

Touchpad PG 43

CIR PG 42

T/P Board CIR Board

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DELL/FLEX CONFIDENTIAL

Title		
BLOCK DIAGRAM		
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Power States									
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off	
+PWR_SRC	N/A	V	V	V	V				
+0.75V_DDR_VTT	RUN_ON/SUS_ON	V	V						
+V1.1S_VTT	+V1.1S_VTT_MXM1_PWRON	V							
+V1.1S	RUN_ON	V							
+1.5V_RUN	RUN_ON#	V							
+1.5V_DDR	RUN_ON/SUS_ON	V	V						
+V1.8S	RUN_ON	V							
+3.3V_ALW	3VA_PCH_ON	V	V	V	V				
+3.3V_WLAN	AUX_EN_WOWL	V	define WOL	define WOL	define WOL				
+3.3V_RUN	RUN_ON#	V							
+V3.3	SUS_ON	V	V						
+5V_ALW	+5V_EN1/5V_ALW_ON	V	V	V	V				
+5V_ALW2	+PWR_SRC	V	V	V	V				
+5V_RUN	RUN_ON	V							
+5V_HDD	HDDC_EN	V							
+5V_MOD	MODC_EN	V							
+V5S	RUN_ON	V							
+LCDVCC	ENVDD	V							
+RTC_CELL	RTC	V	V	V	V	V			
+VCC_CORE	IMVP_VR_ON	V							
+USB_RIGHT_PWR	USB_SIDE_EN#	V	define	define					
+USB_LEFT_PWR	USB_BACK_EN#	V	define	define					
+15V_ALW	5V_ALW_ON	V	V	V	V				
+3.3V_ALW_17020	+3.3V_EN2/5V_ALW_ON	V	V	V	V				
+V3.3M_LAN	PM_SLP_LAN#	V	define WOL	define WOL	define WOL				

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FRONTPAGE		
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Clarksfield / Auburndale

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XDP port

SA_CK0
SA_CK1

SO-DIMM 1

SB_CK0
SB_CK1

SO-DIMM 2

BCLK_ITP_P / BCLK_ITP
BCLK_ITP_N / BCLK_ITP#

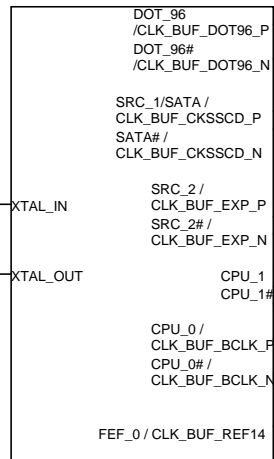
CLK_EXP_P / PEG_CLK
CLK_EXP_N / PEG_CLK#

BCLK / BCLK_CPU_P
BCLK# / BCLK_CPU_N

IBex-Peak

CLK_EXP_P / CLKOUT_DMI_P
CLK_EXP_N / CLKOUT_DMI_N

ICS9LRS3191AKLFT CLK GEN



CLKOUT_PCIE0N / CLK_PCIE_EXPCARD#
CLKOUT_PCIE0P / CLK_PCIE_EXPCARD

CLKOUT_PCIE1N / CLK_PCIE_MINI1#
CLKOUT_PCIE1P / CLK_PCIE_MINI1

CLKOUT_PCIE2N / CLK_PCIE_MINI2#
CLKOUT_PCIE2P / CLK_PCIE_MINI2

CLKOUT_PCIE3N / CLK_PCIE_MINI3#
CLKOUT_PCIE3P / CLK_PCIE_MINI3

CLKOUT_PCIE4N / CLK_PCH_SRC4_N
CLKOUT_PCIE4P / CLK_PCH_SRC4_P

CLKOUT_PCIE5N / NC_CLK_PCH_SRC5_N
CLKOUT_PCIE5P / NC_CLK_PCH_SRC5_P

CLKOUT_PEG_A_N / CLK_PCIE_VGA1#
CLKOUT_PEG_A_P / CLK_PCIE_VGA1

CLKOUT_PEG_B_N / CLK_PCIE_VGA2#
CLKOUT_PEG_B_P / CLK_PCIE_VGA2

SML0CLK / SML0_CLK
SML0DATA / SML0_DATA

SML1CLK / SMBCLK2
SML1DATA / SMBCLK2

CLKOUT_PCIE10 / CLK_PCH_PCCARD

CLKOUT_PCIE11 / CLK_PCH_FB
CLKIN_PCH_LOOPBACK / CLK_PCH_FB#

JTAG_TCK / PCH_XDP_TCLK

CLKOUT_PCIE12 / CLK_LPC
CLKOUT_PCIE12 / CLK_LPC_DEBUG

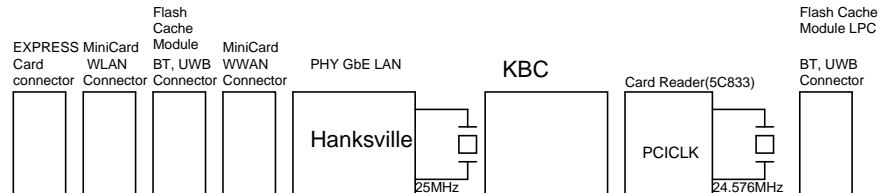
CLKOUT_PCIE13

TEST PAD

MXM-III 3.0 1

MXM-III 3.0 2

Debug Port



Hanksville

KBC

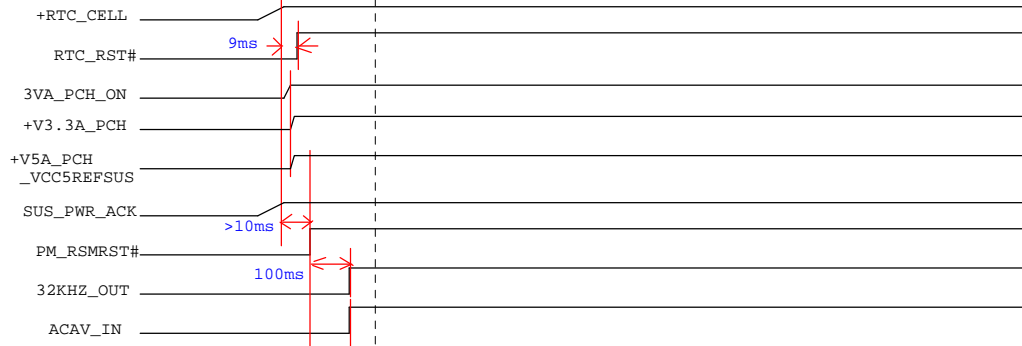
Card Reader(5C833)

Flash Cache Module LPC

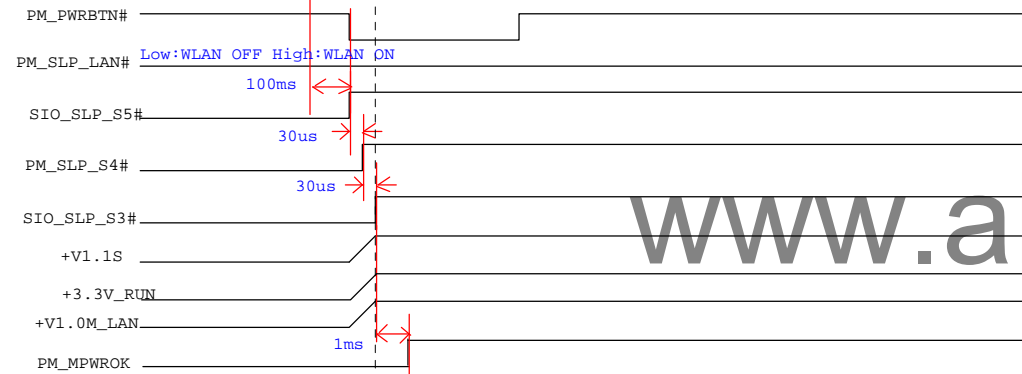
BT, UWB Connector

Title			
CLOCK MAP			
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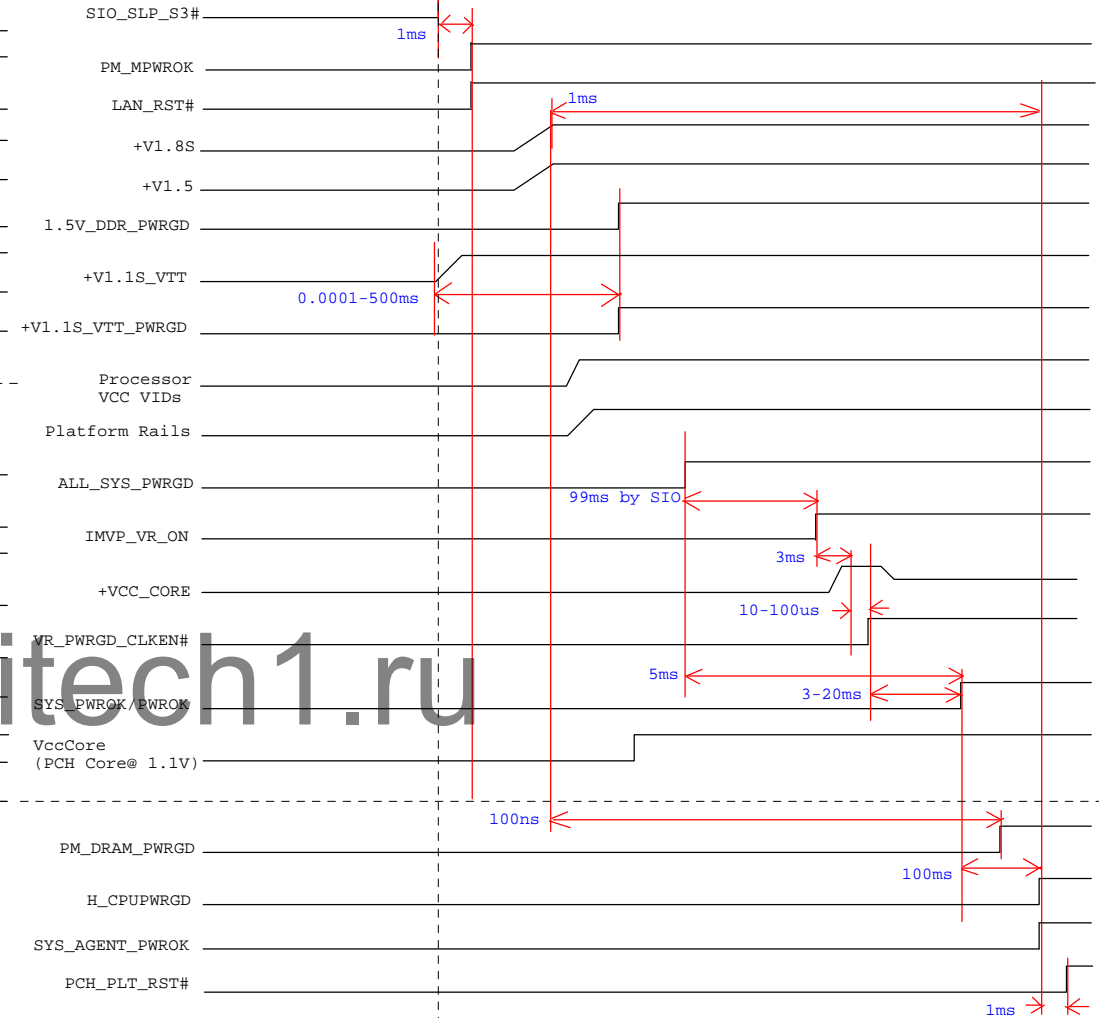
G3 to Sx



Sx to S0



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Title		
POWER SEQUENCING		
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VDD_I/O can be ranging from 1.05V to 3.3V.

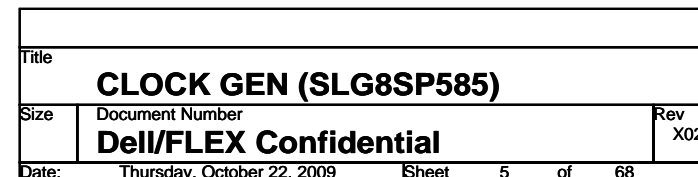
40mil width every power pin.

L18
BLM18AG121SN1D
L0603
2 1

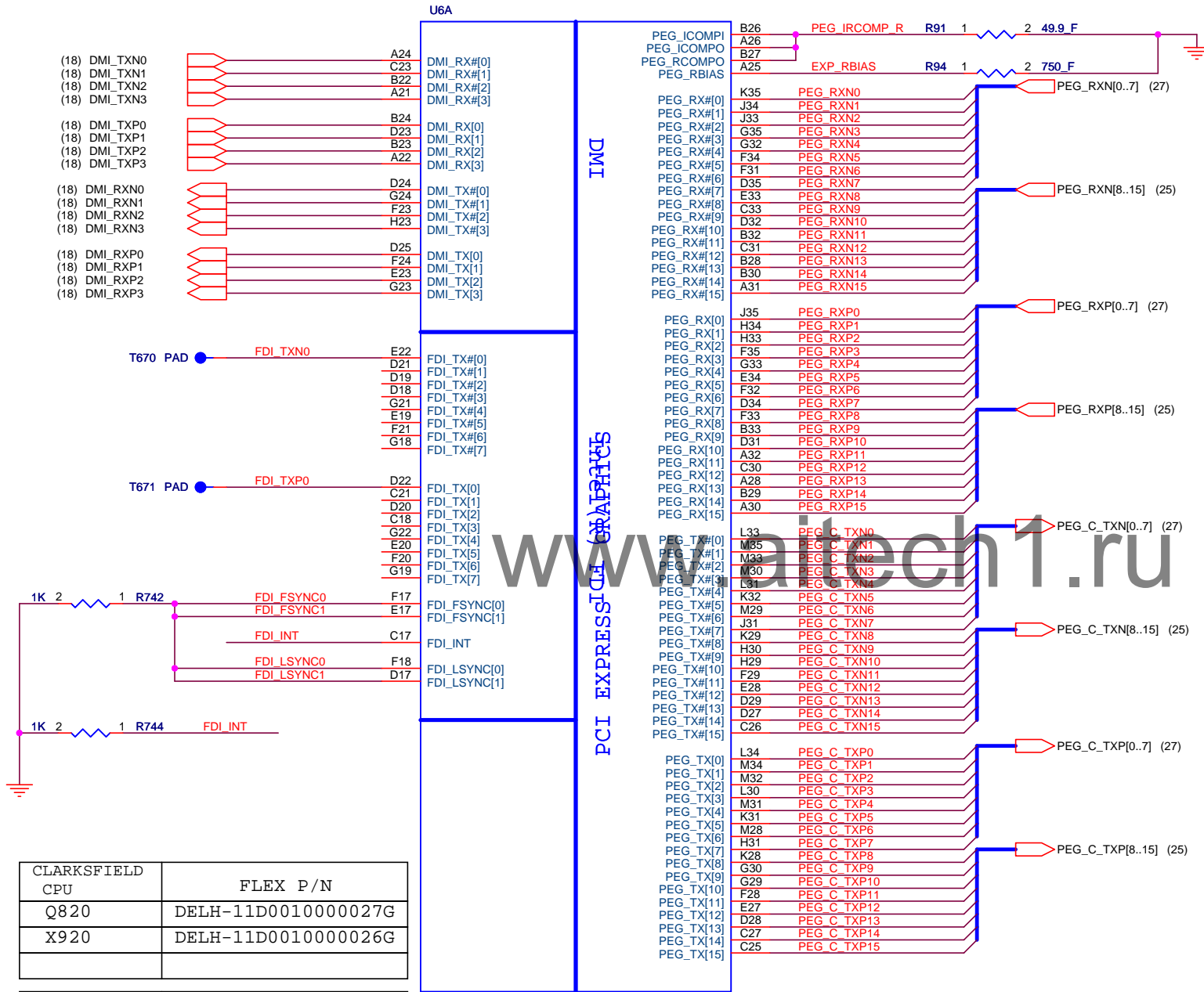
L19
*BLM18AG121SN1D_NC
L0603
2 1

+V1.1S

+3.3V_RUN



ARRANDALE /CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



www.aitech1.ru

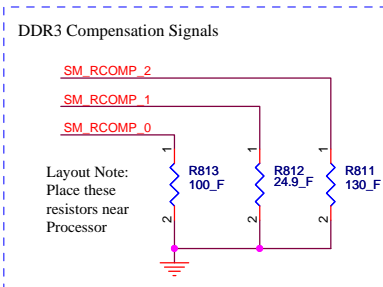
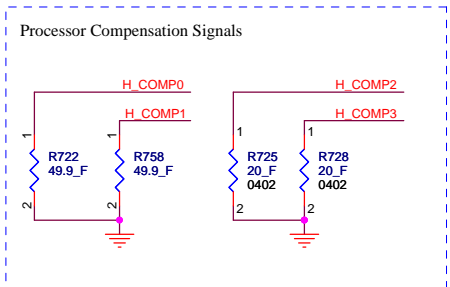
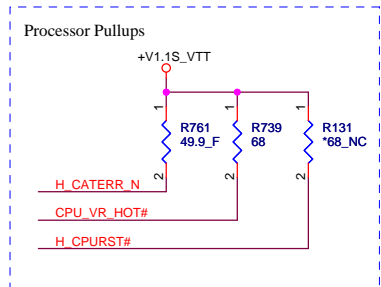
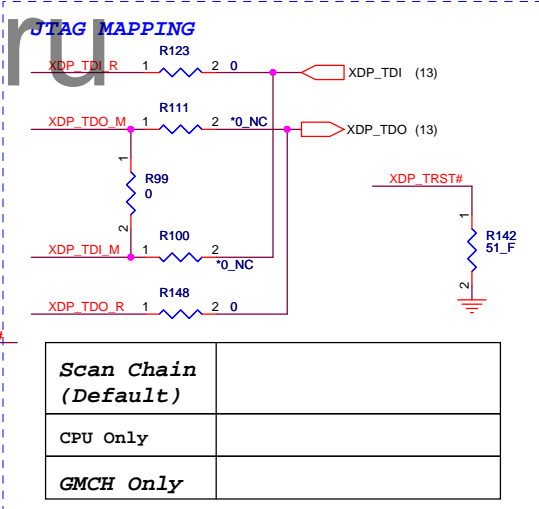
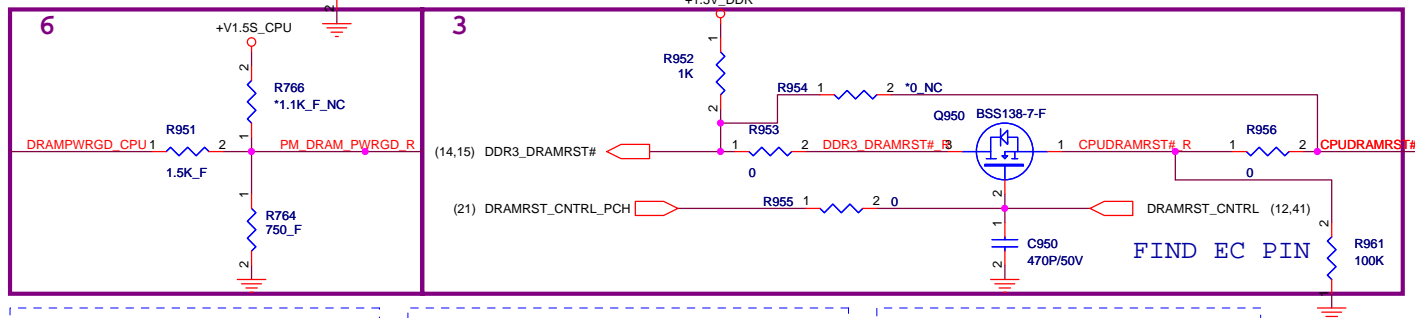
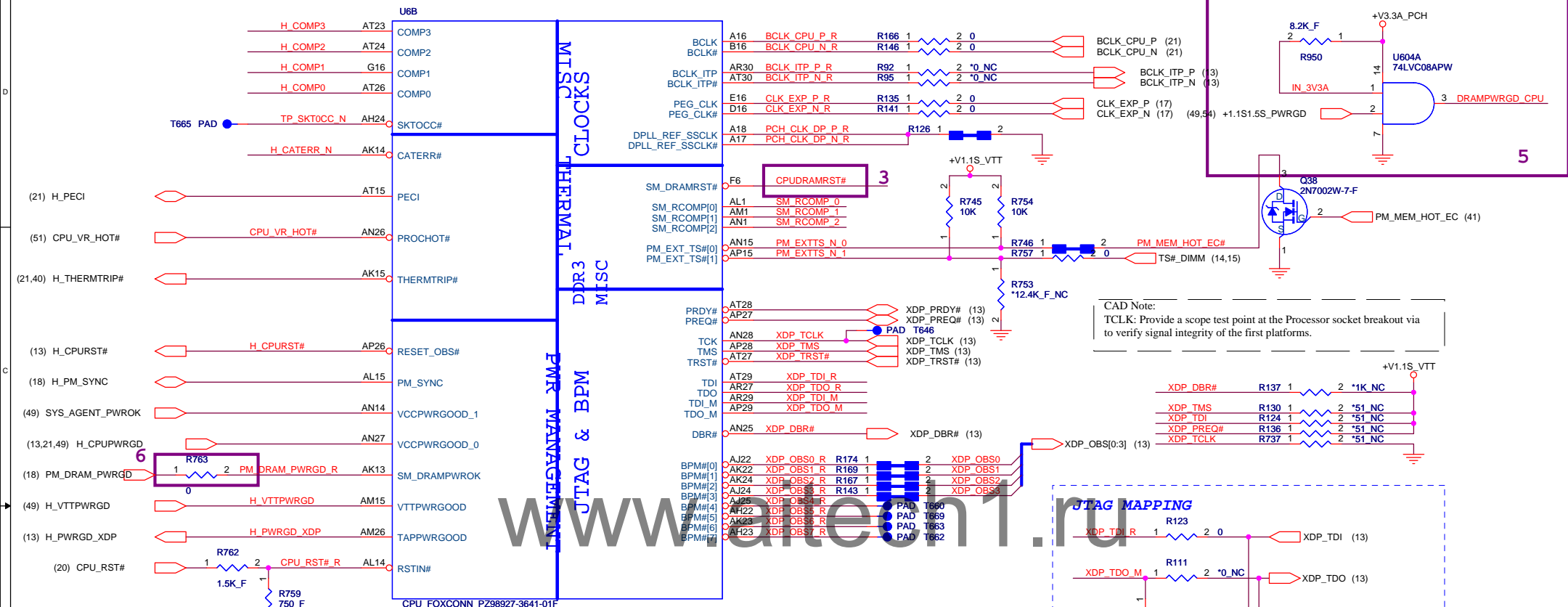
CLARKSFIELD CPU	FLEX P/N
Q820	DELH-11D0010000027G
X920	DELH-11D0010000026G

Arrandale CPU	FLEX P/N
520M	DELH-11D0010000037G

CPU_FOXCONN_PZ98927-3641-01F

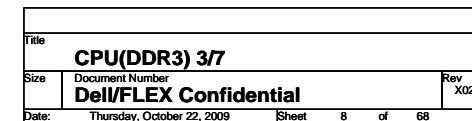
Title	
CPU (DMI,PEG,FDI) 1/7	
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Dell/FLEX Confidential	

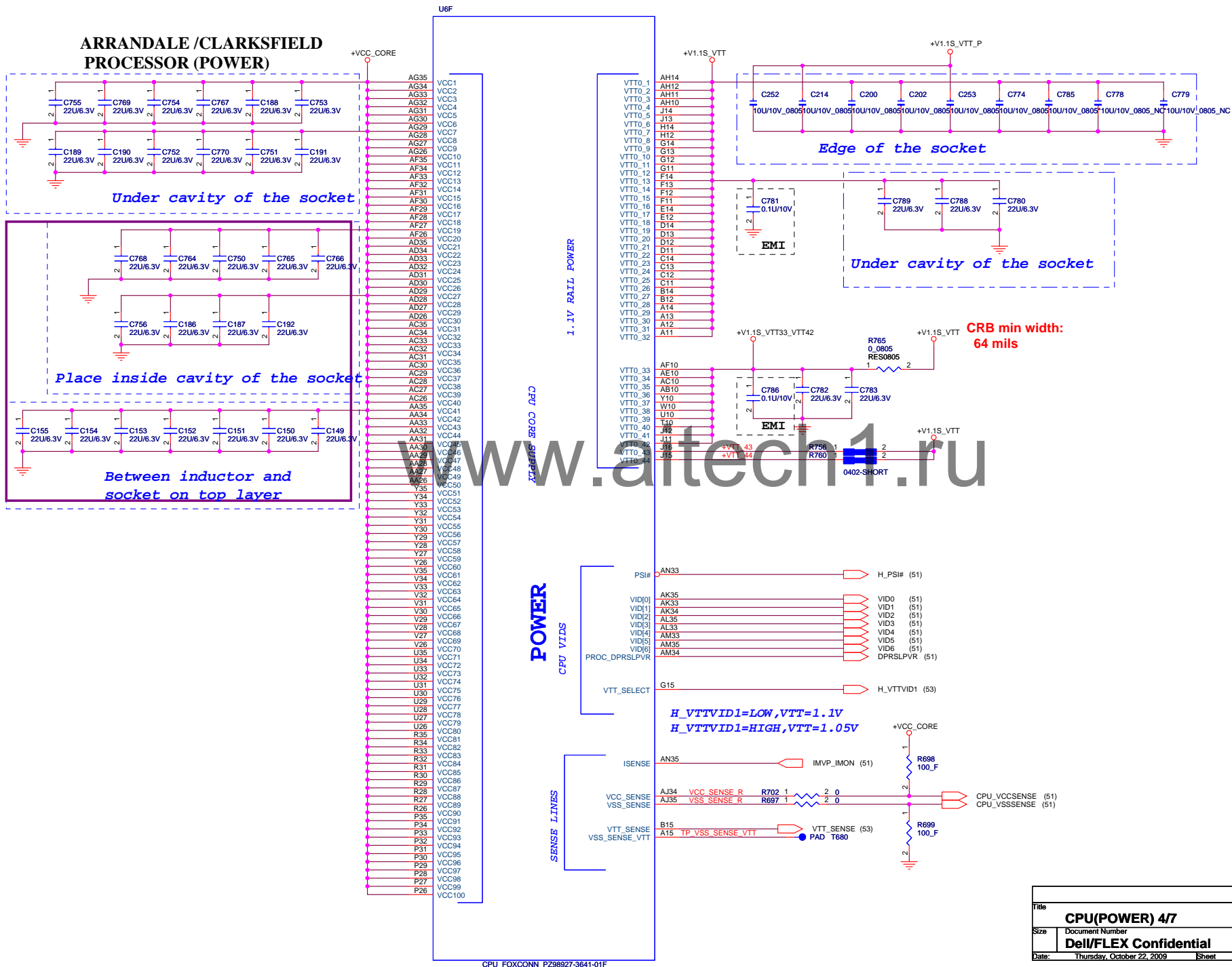
ARRANDALE / CLARKSFIELD PROCESSOR (CLK, MISC, JTAG)



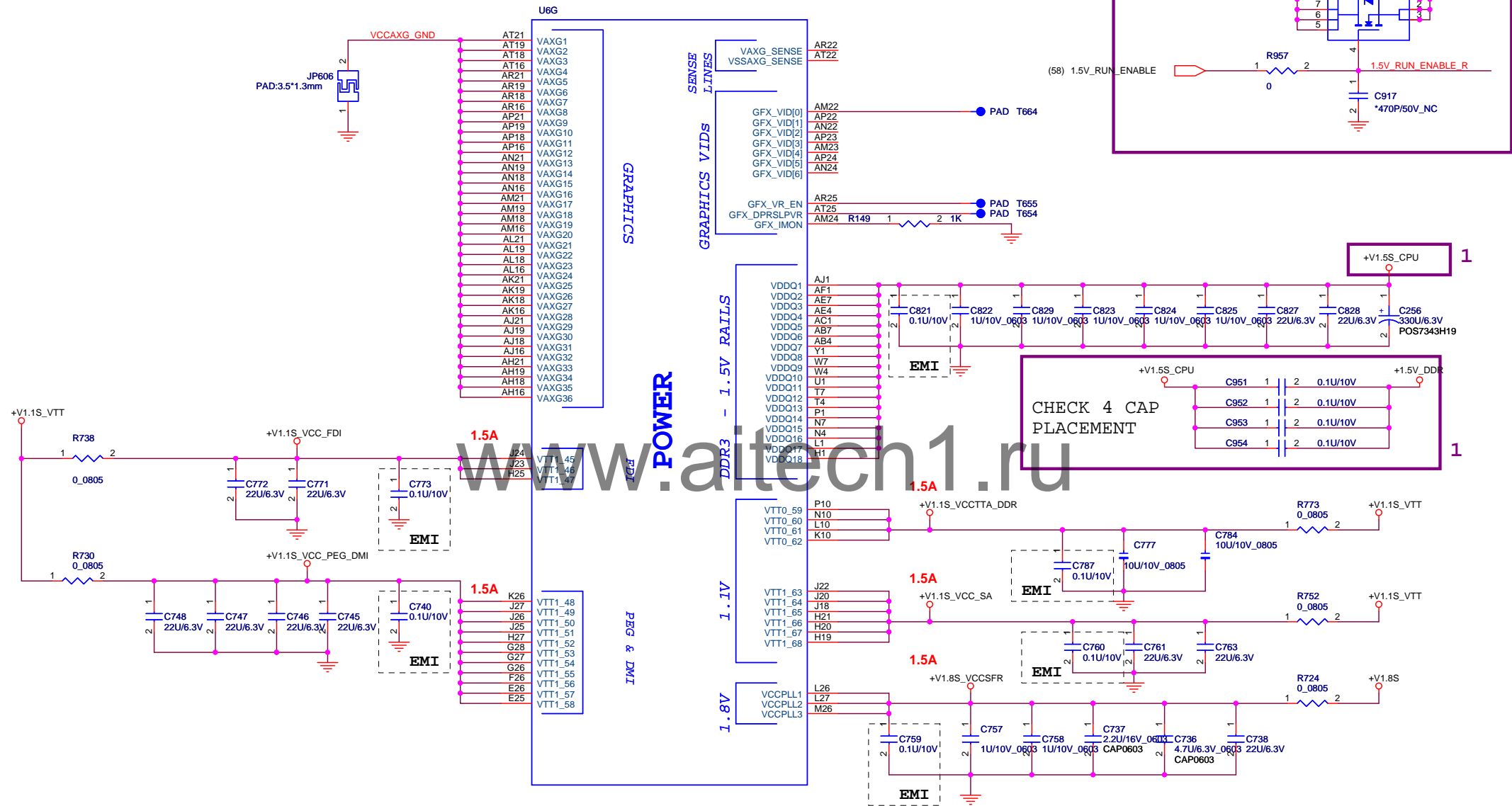
<i>Scan Chain (Default)</i>	
CPU Only	
<i>GMCH Only</i>	

Diagram illustrating the mapping of memory addresses to cache lines. The left side shows a list of memory addresses (SA_DQS#1 to SA_DQS#7) and their corresponding cache lines (J9, N9, AH7, AK9, AP11, AT13). The right side shows a list of memory addresses (M_B_DQ33 to M_B_DQ49) and their corresponding cache lines (AG1, AJ3, AK1, AG4, AG3, AJ4, AH4, AK3, AK4, AN6, AN2, AK5, AK2, AM4, AK3, AP3, AN5). A red arrow points from the left side to the right side, indicating a mapping from SA_DQS#7 to M_B_DQ49.





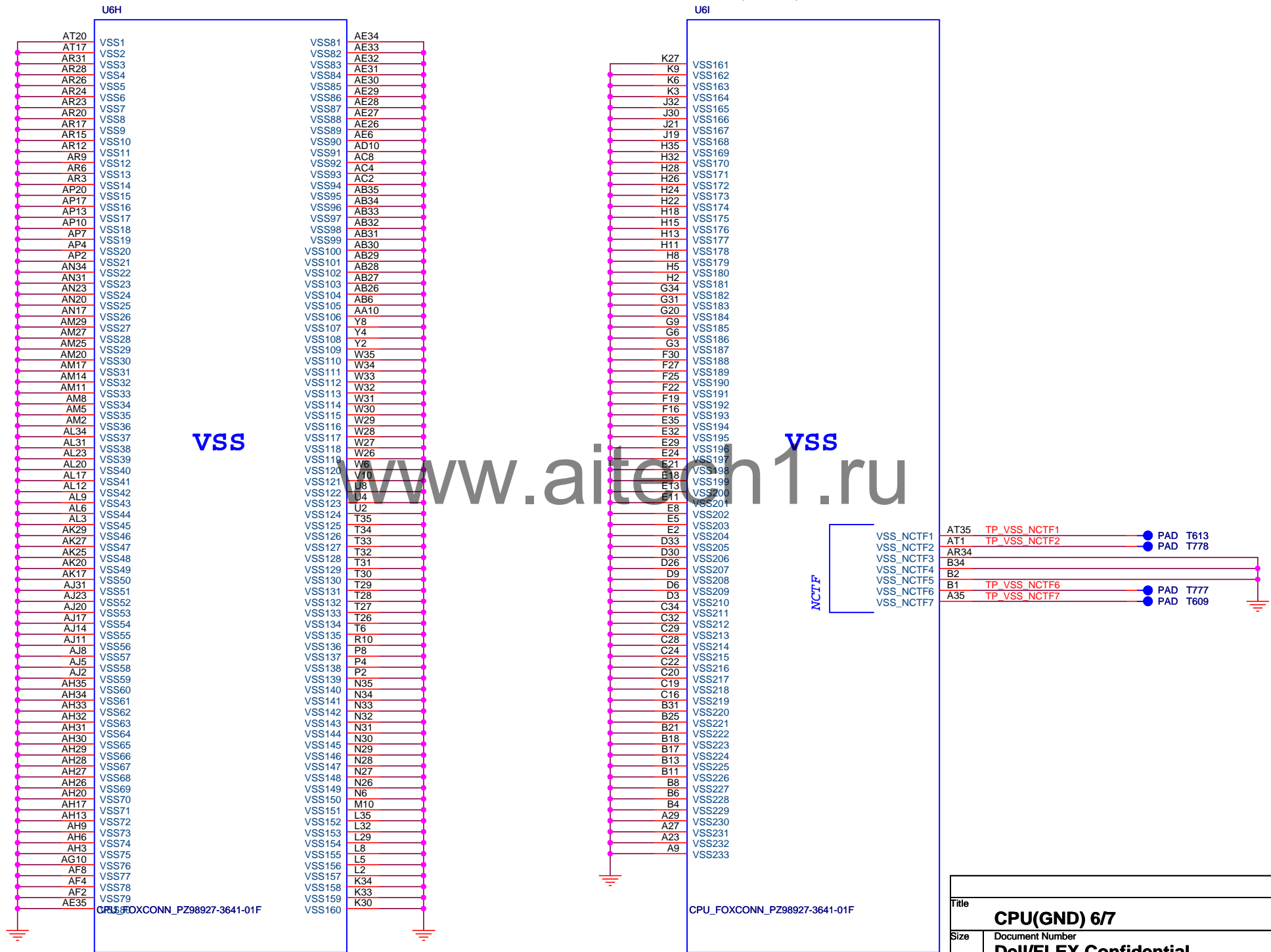
ARRANDALE /CLARKSFIELD PROCESSOR (GRAPHICS POWER)



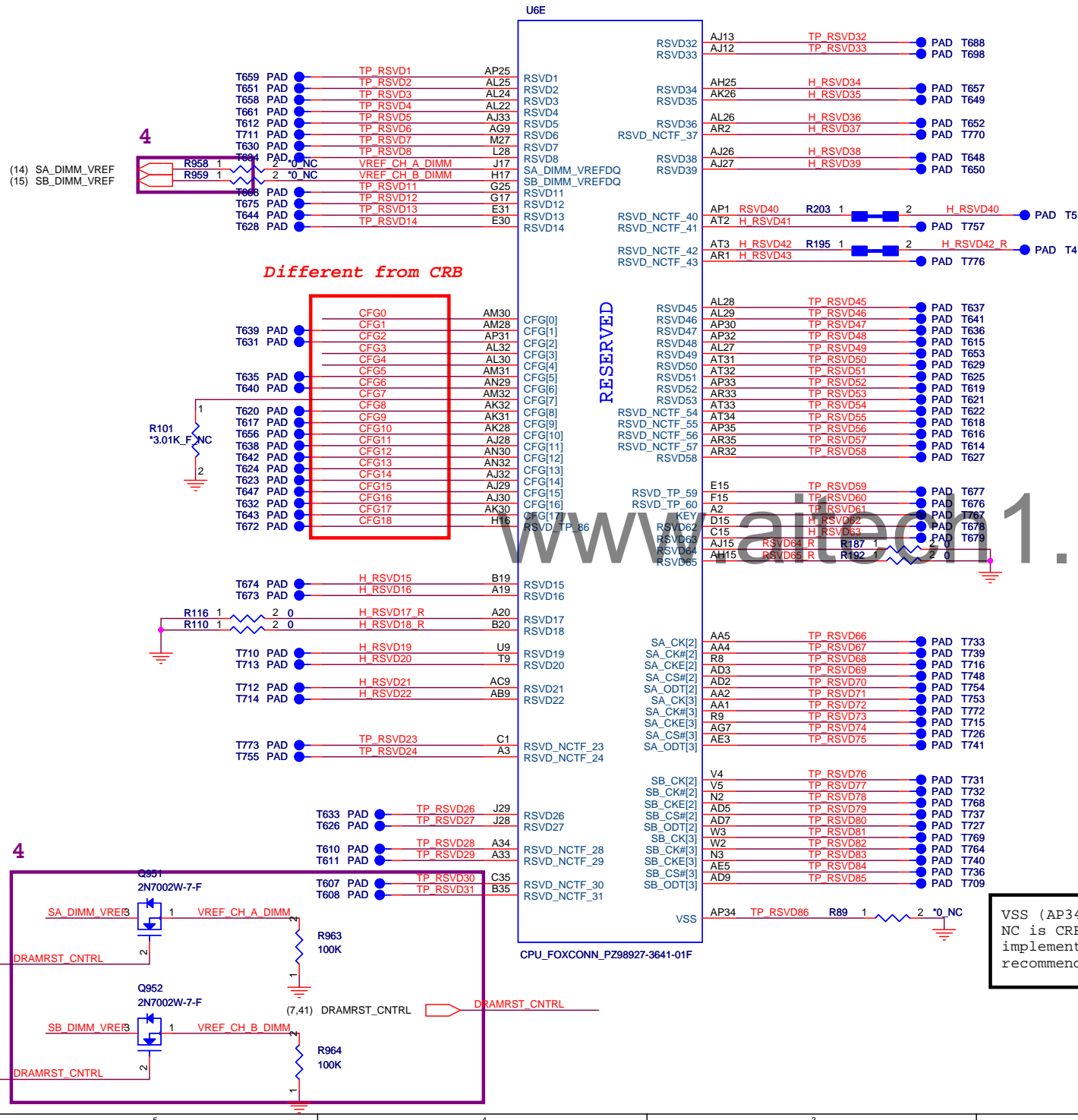
CPU_FOXCONN_PZ98927-3641-01F

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CPU (GRAPHICS PWR) 5/7			
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ARRANDALE /CLARKSFIELD PROCESSOR (GND)

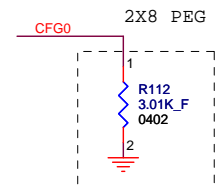


ARRANDALE /CLARKSFIELD PROCESSOR(RESERVED, CFG)

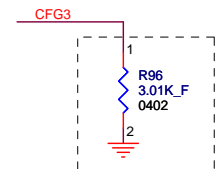


CFG Straps for PROCESSOR

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled



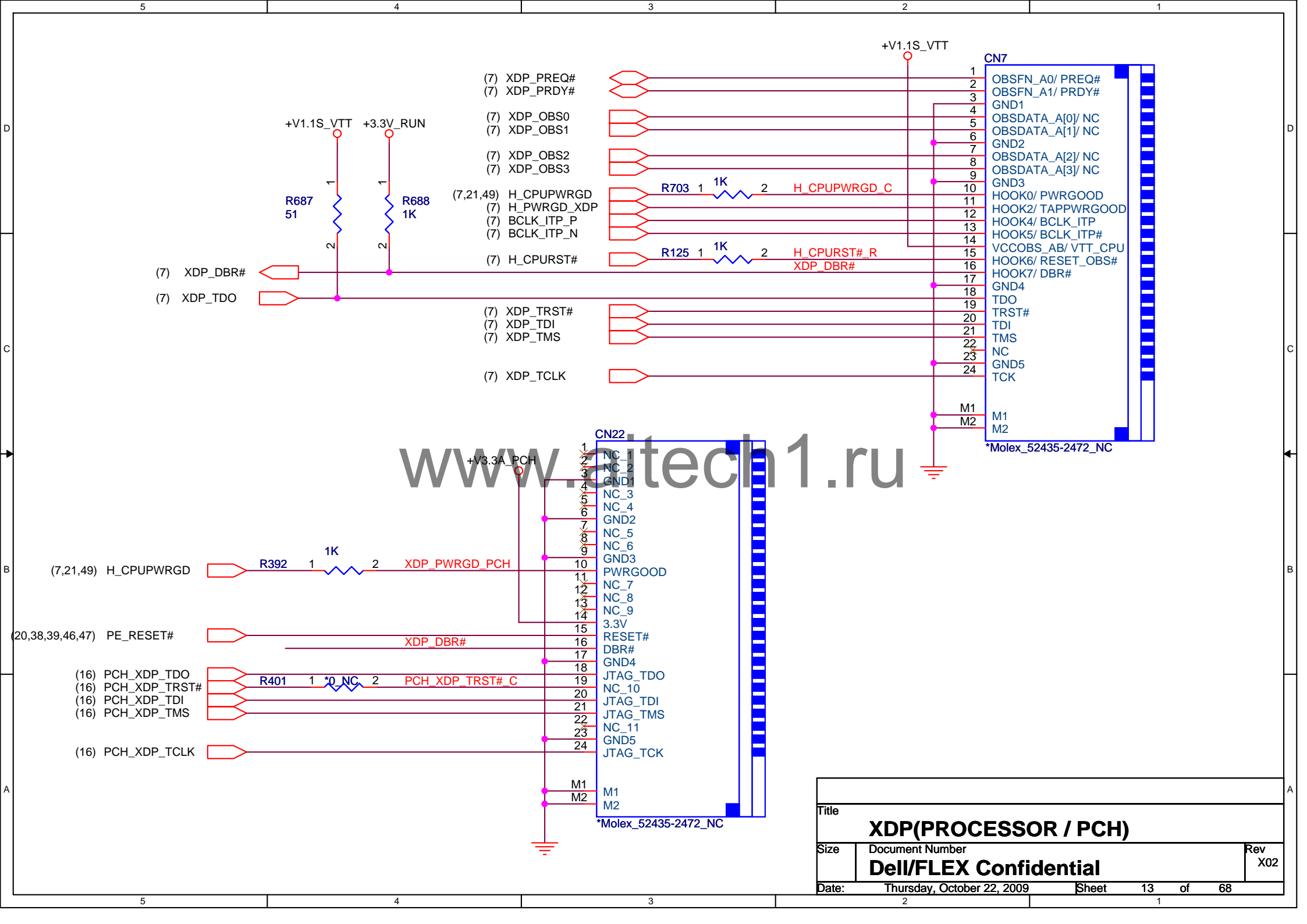
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



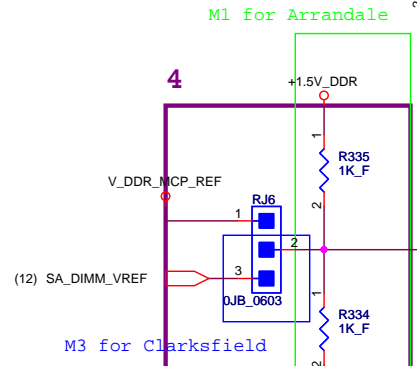
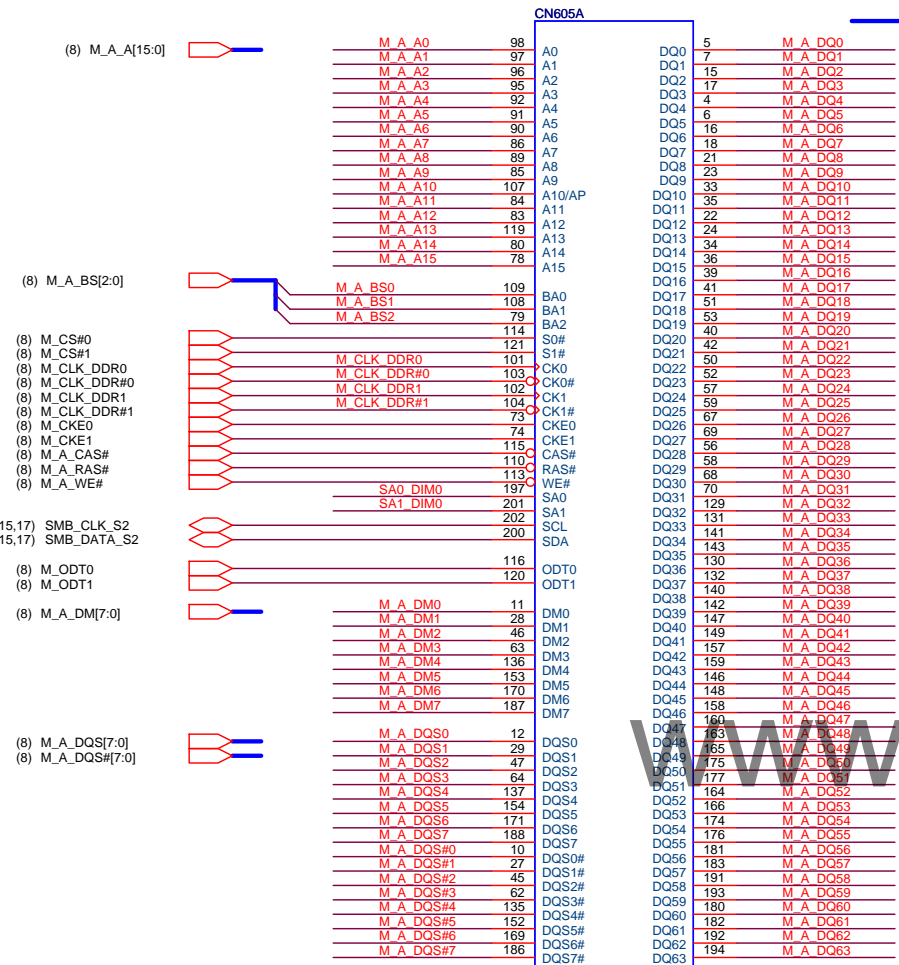
CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port (Default)</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port</p>



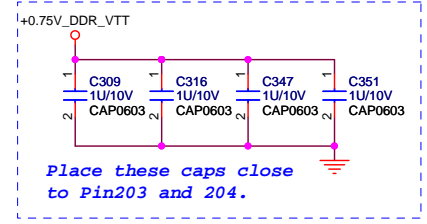
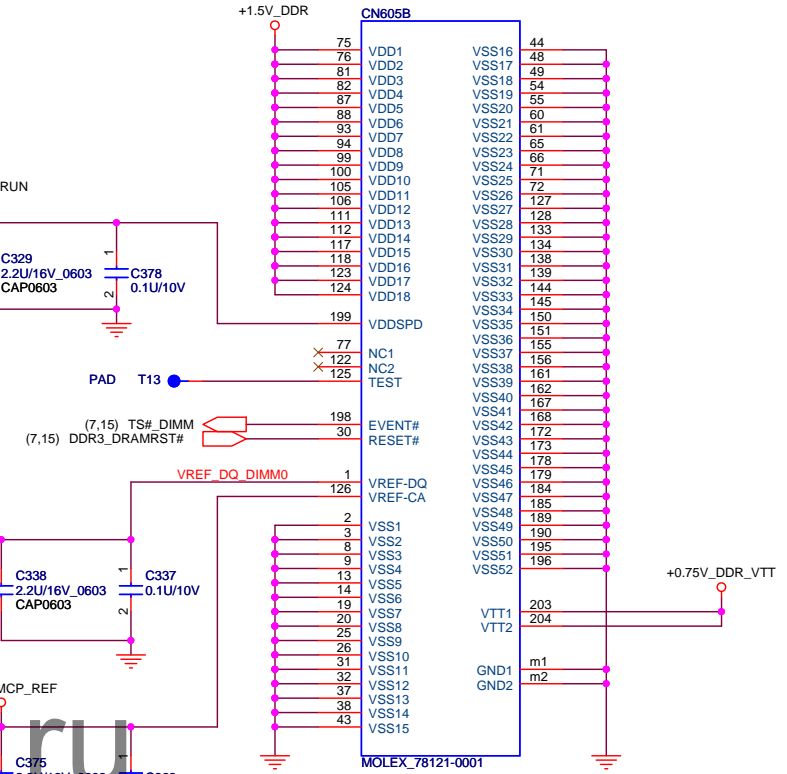
VSS (AP34) can be left
NC is CRB
implementation; EDS/DG
recommendation to GND



Title		
XDP(PROCESSOR / PCH)		
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DESIGN 1.6 showed that both M1 and M3 should be concurrently implemented for both CPU



Layout Note:
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin (9/9).

SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM0 = 1, SA1_DIM0 = 0	SPD	0xA2
	TS	0x32

(8) M_B_A[15:0]

(8) M_B_BS[2:0]

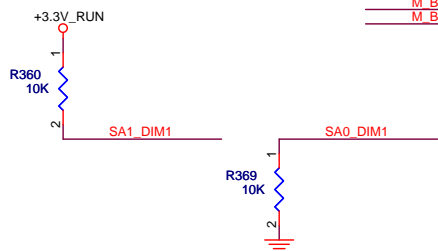
(8) M_CS#2
(8) M_CS#3
(8) M_CLK_DDR2
(8) M_CLK_DDR#2
(8) M_CLK_DDR3
(8) M_CLK_DDR#3
(8) M_CKE2
(8) M_CKE3
(8) M_B_CAS#
(8) M_B_RAS#
(8) M_B_WE#

(5,14,17) SMB_CLK_S2
(5,14,17) SMB_DATA_S2

(8) M_ODT2
(8) M_ODT3

(8) M_B_DM[7:0]

(8) M_B_DQS[7:0]
(8) M_B_DQS#7[0]



SO-DIMM Address

SPD	0xA4
TS	0x34

M B A0 98
M B A1 97
M B A2 96
M B A3 95
M B A4 92
M B A5 91
M B A6 90
M B A7 89
M B A8 88
M B A9 85
M B A10 107
M B A11 84
M B A12 83
M B A13 119
M B A14 80
M B A15 78

M B BS0 109
M B BS1 108
M B BS2 79
M CLK_DDR2 101
M CLK_DDR#2 103
M CLK_DDR3 102
M CLK_DDR#3 104
CKE0 73
CKE1 74
CAS# 115
RAS# 119
WE# 197
SA0_DIM1 201
SA1_DIM1 202
SCL 200
SDA 116
ODT0 120
ODT1 120

M B DM0 11
M B DM1 28
M B DM2 46
M B DM3 63
M B DM4 136
M B DM5 153
M B DM6 170
M B DM7 187

M B DQS0 12
M B DQS1 29
M B DQS2 47
M B DQS3 64
M B DQS4 137
M B DQS5 154
M B DQS6 171
M B DQS7 188
M B DQS#0 10
M B DQS#1 27
M B DQS#2 45
M B DQS#3 62
M B DQS#4 135
M B DQS#5 152
M B DQS#6 169
M B DQS#7 186

MOLEX_78192-0001

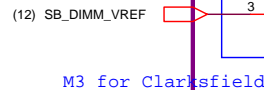
CN606A

A0 5
A1 7
A2 15
A3 17
A4 4
A5 6
A6 16
A7 18
A8 21
A9 23
A10/AP 33
A11 35
A12 22
A13 24
A14 34
A15 36
BA0 41
BA1 51
BA2 53
S0# 40
S1# 42
CK0 50
CK0# 52
CK1 57
CK1# 59
CKE0 67
CKE1 69
CAS# 56
RAS# 58
WE# 68
SA0 70
SA1 129
SCL 131
SDA 141
ODT0 143
ODT1 130
DM0 142
DM1 147
DM2 149
DM3 157
DM4 159
DM5 146
DM6 148
DM7 168
DQS0 163
DQS1 165
DQS2 175
DQS3 177
DQS4 164
DQS5 166
DQS6 174
DQS7 176
DQS#0 181
DQS#1 183
DQS#2 191
DQS#3 193
DQS#4 180
DQS#5 182
DQS#6 192
DQS#7 194

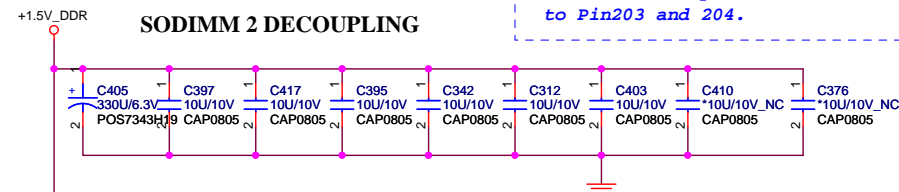
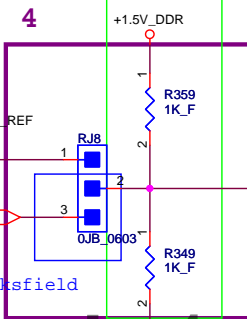
M B DQ0 5
M B DQ1 7
M B DQ2 15
M B DQ3 17
M B DQ4 4
M B DQ5 6
M B DQ6 16
M B DQ7 18
M B DQ8 21
M B DQ9 23
M B DQ10 33
M B DQ11 35
M B DQ12 22
M B DQ13 24
M B DQ14 34
M B DQ15 36
M B DQ16 39
M B DQ17 41
M B DQ18 51
M B DQ19 53
M B DQ20 40
M B DQ21 42
M B DQ22 50
M B DQ23 52
M B DQ24 57
M B DQ25 59
M B DQ26 67
M B DQ27 69
M B DQ28 56
M B DQ29 58
M B DQ30 68
M B DQ31 70
M B DQ32 129
M B DQ33 131
M B DQ34 141
M B DQ35 143
M B DQ36 130
M B DQ37 132
M B DQ38 140
M B DQ39 142
M B DQ40 147
M B DQ41 157
M B DQ42 159
M B DQ43 146
M B DQ44 148
M B DQ45 168
M B DQ46 163
M B DQ47 165
M B DQ48 175
M B DQ49 177
M B DQ50 164
M B DQ51 166
M B DQ52 174
M B DQ53 176
M B DQ54 181
M B DQ55 183
M B DQ56 191
M B DQ57 193
M B DQ58 180
M B DQ59 182
M B DQ60 192
M B DQ61 194
M B DQ62 194
M B DQ63 194

DESIGN 1.6 showed that both M1 and M3 should be con-currently implemented for both CPU

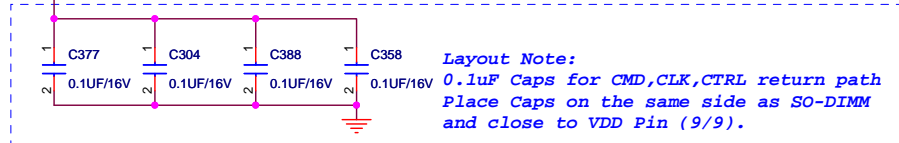
M1 for Arrandale
M3 for Clarksfield



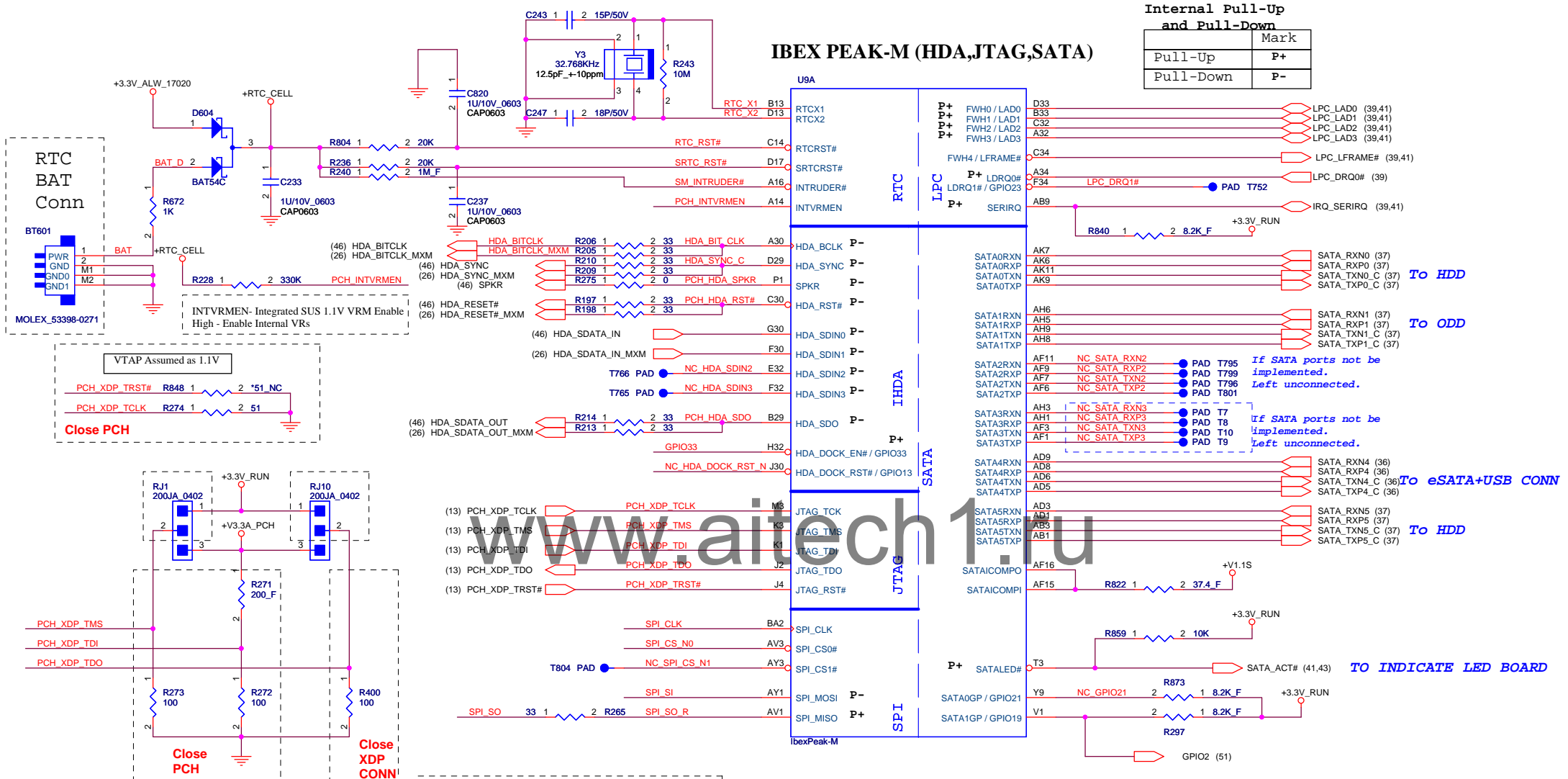
M1 for Arrandale



SODIMM 2 DECOUPLING



Layout Note:
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin (9/9).



Internal Pull-Up and Pull-Down

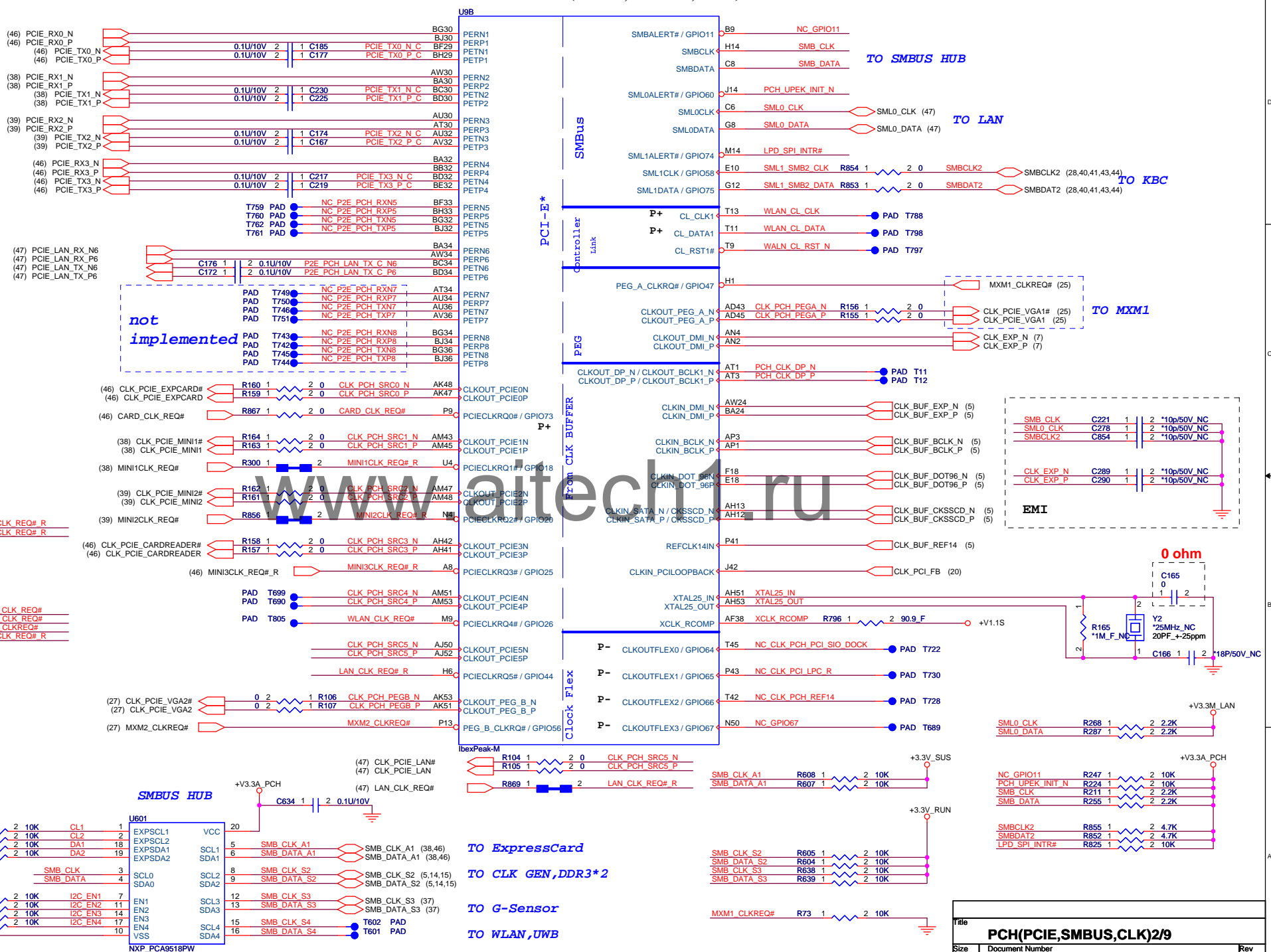
	Mark
Pull-Up	P+
Pull-Down	P-

Flash Descriptor Security

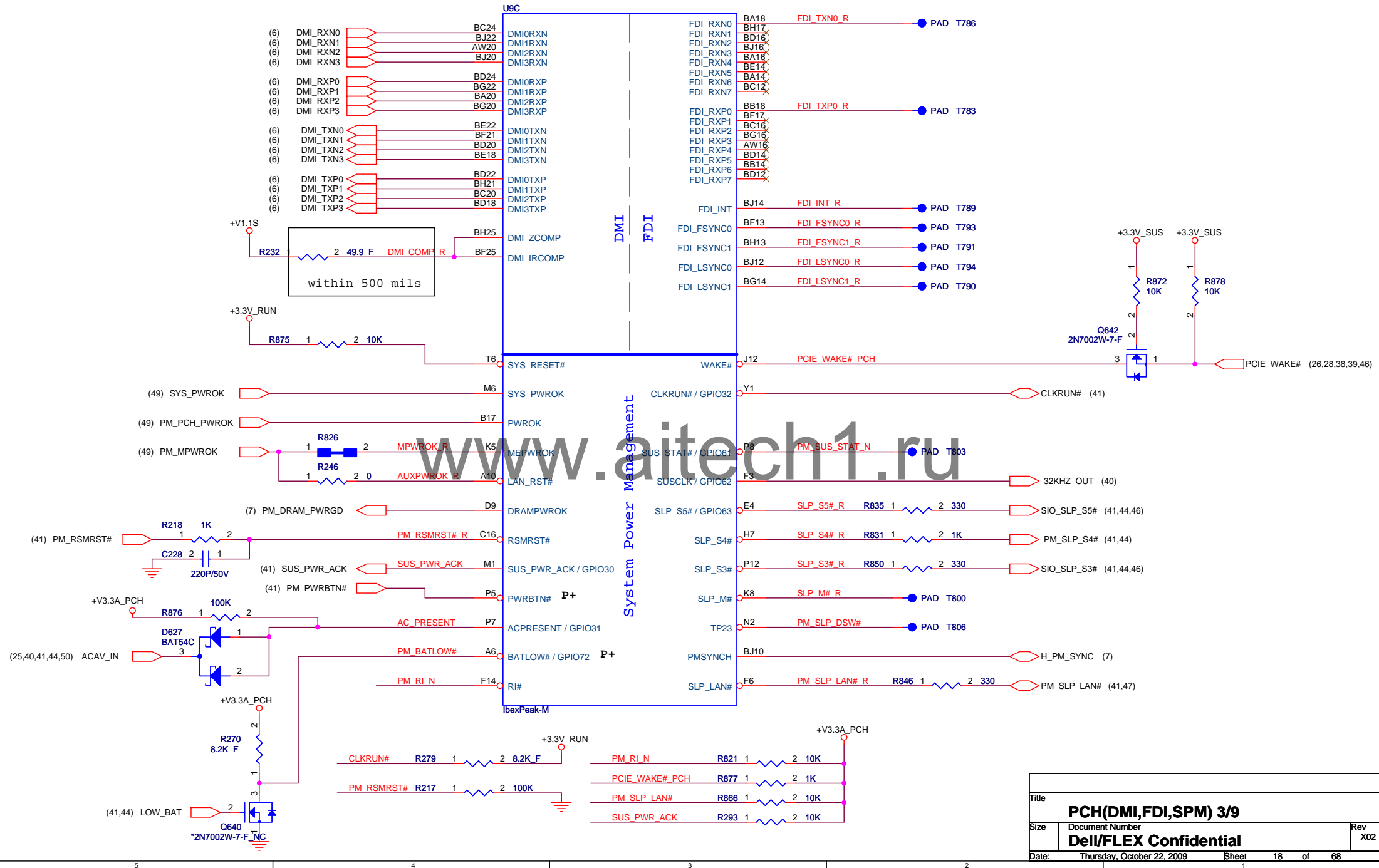
High	Flash Descriptor will be in effect (default)
Low	Descriptor Security will be overridden

IBEX PEAK-M (PCI-E,SMBUS,CLK)

PCI-E* x1	Usage
Lane 1	Express Card
Lane2	WiMax
Lane 3	BT
Lane 4	Card reader/1394
Lane 5	NC
Lane 6	PHY
Lane 7	NC
Lane 8	NC

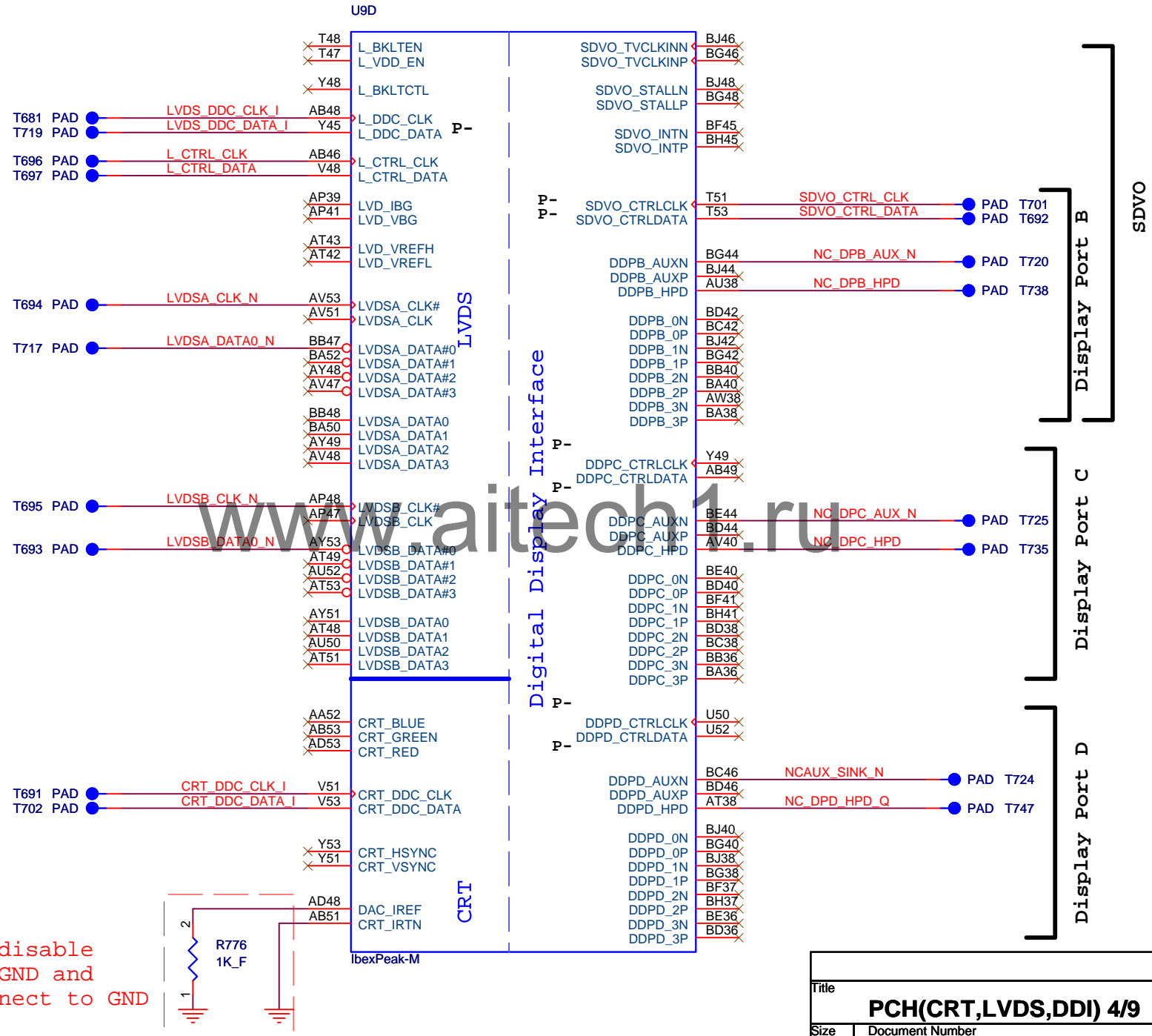


IBEX PEAK-M (DMI,FDI,GPIO)



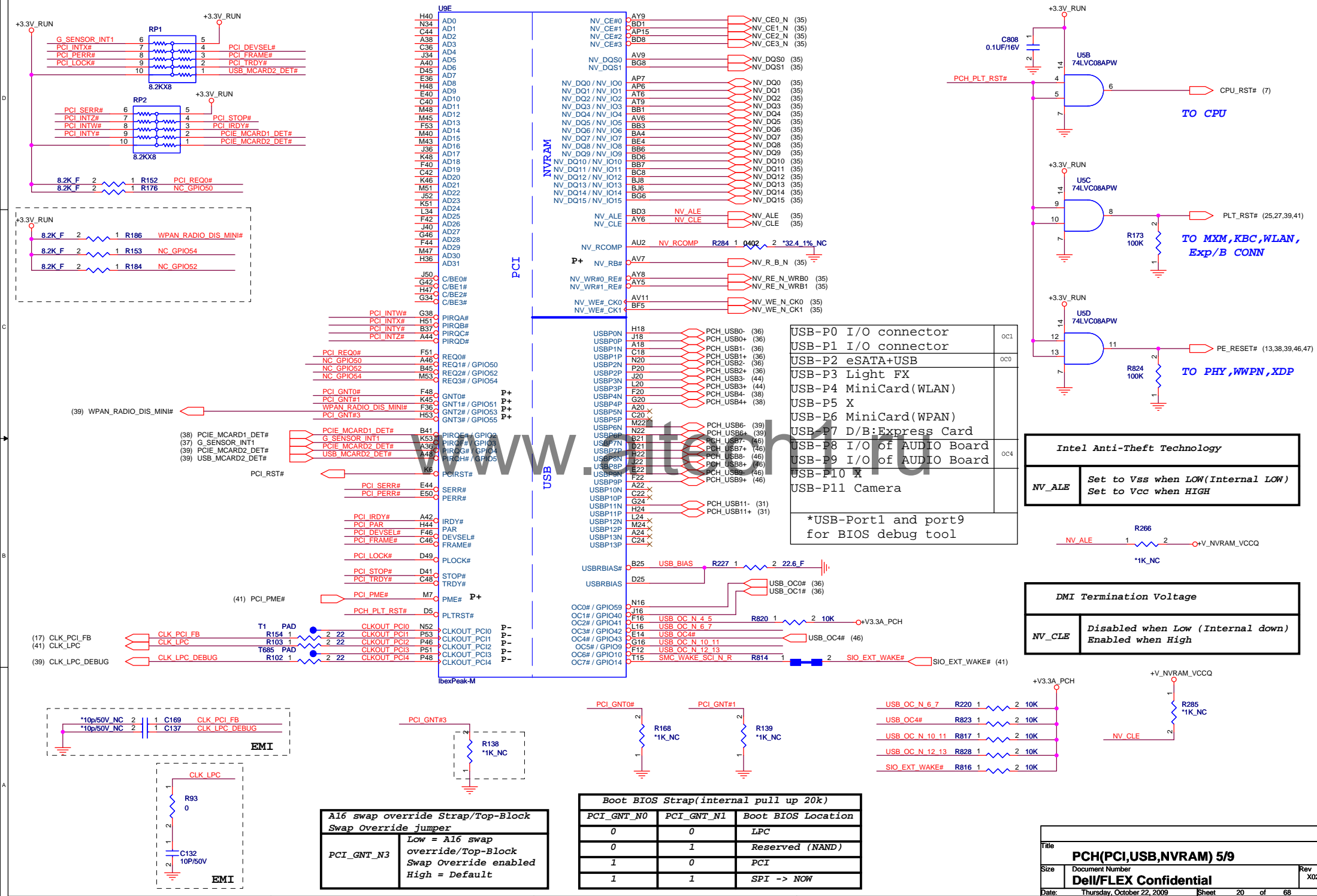
Title		
PCH(DMI,FDI,SPM) 3/9		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
Date:	Thursday, October 22, 2009	Sheet 18 of 68

IBEX PEAK-M (LVDS,DDI)

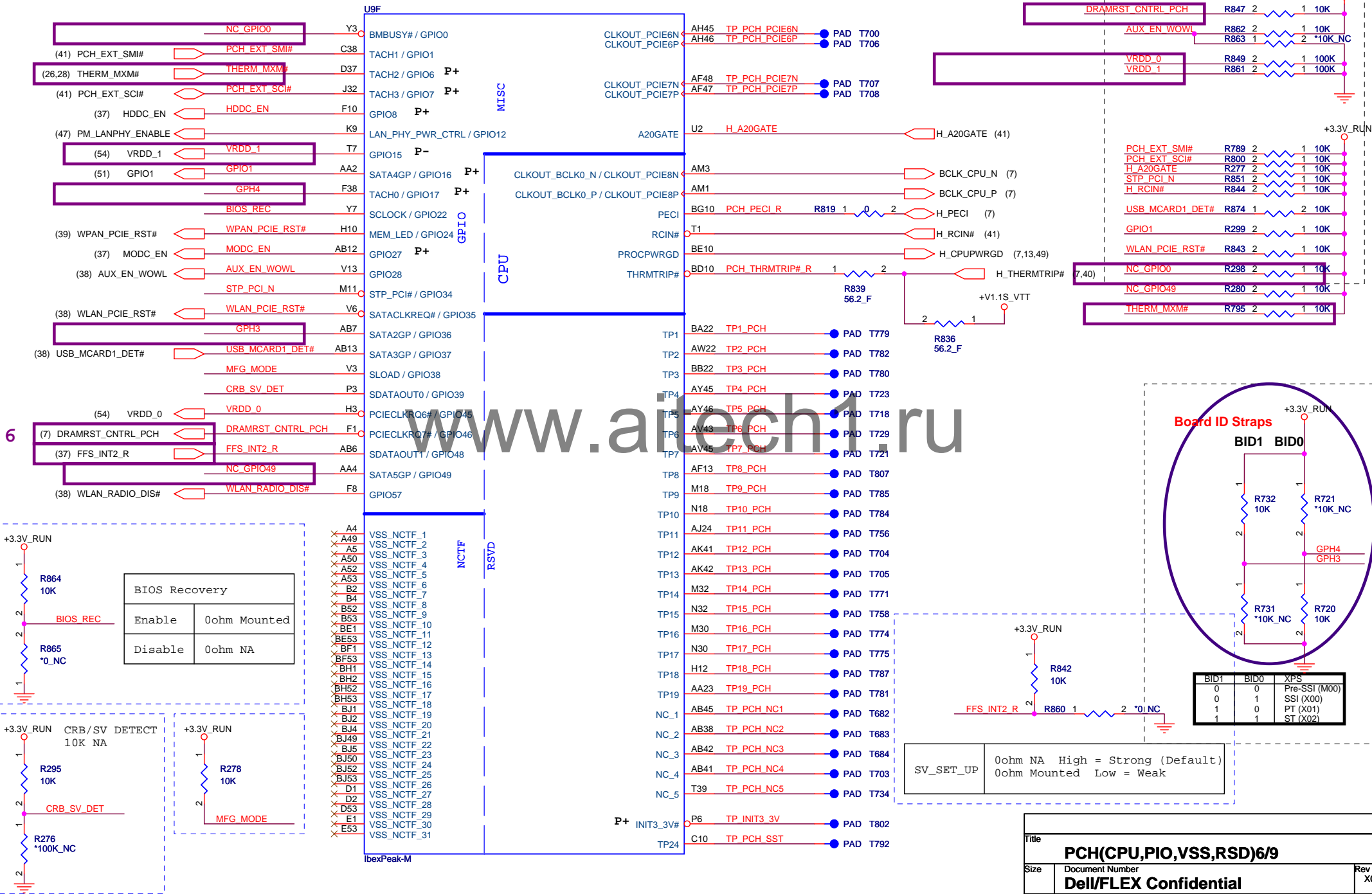


Title		
PCH(CRT,LVDS,DDI) 4/9		
Size	Document Number	Rev
	Dell/FLEX Confidential	X02
Date:	Thursday, October 22, 2009	Sheet 19 of 68

IBEX PEAK-M (PCI,USB,INTEL(R) TURBO MEMORY)

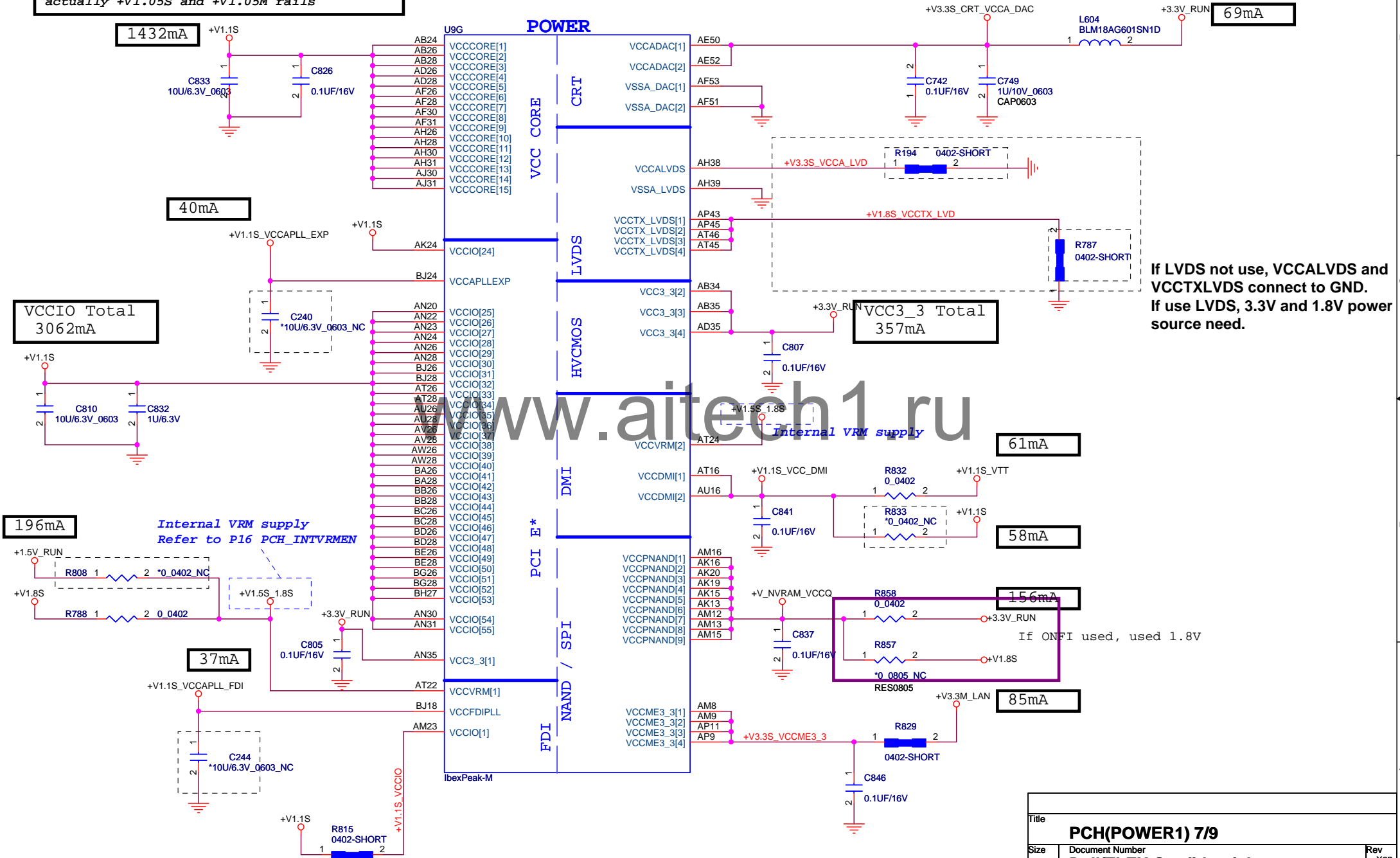


IBEX PEAK-M(GPIO,VSS_NCTF,RSVD)



Please note that all Ibex Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

IBEX PEAK-M(POWER)



IBEX PEAK-M(POWER)

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

VCCIO Total
3062mA

VCCSUS3_3 Total
163mA

VCC3_3 Total
357mA

31mA

6mA

VCCME Total
3062mA

Please note that all Ibex Peak-M rails with netnames +V1.1S and +V1.1M rails are actually +V1.05S and +V1.05M rails

Close to PCH

+5V_ALW has off during S4/S5 battery mode.

<1mA

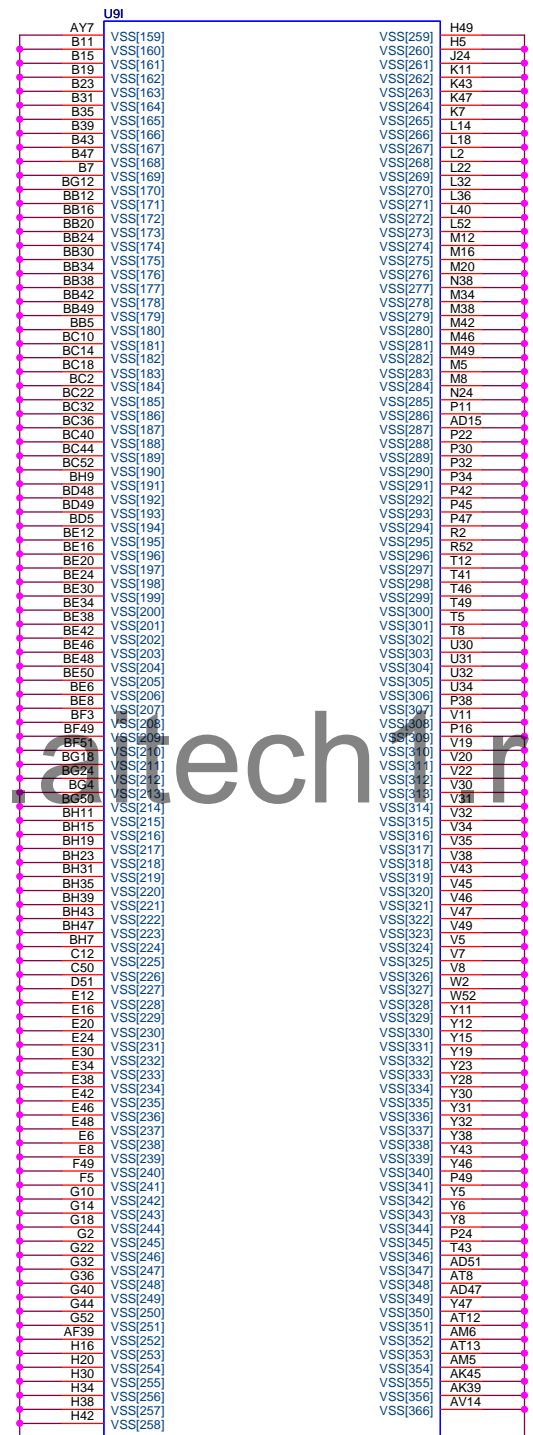
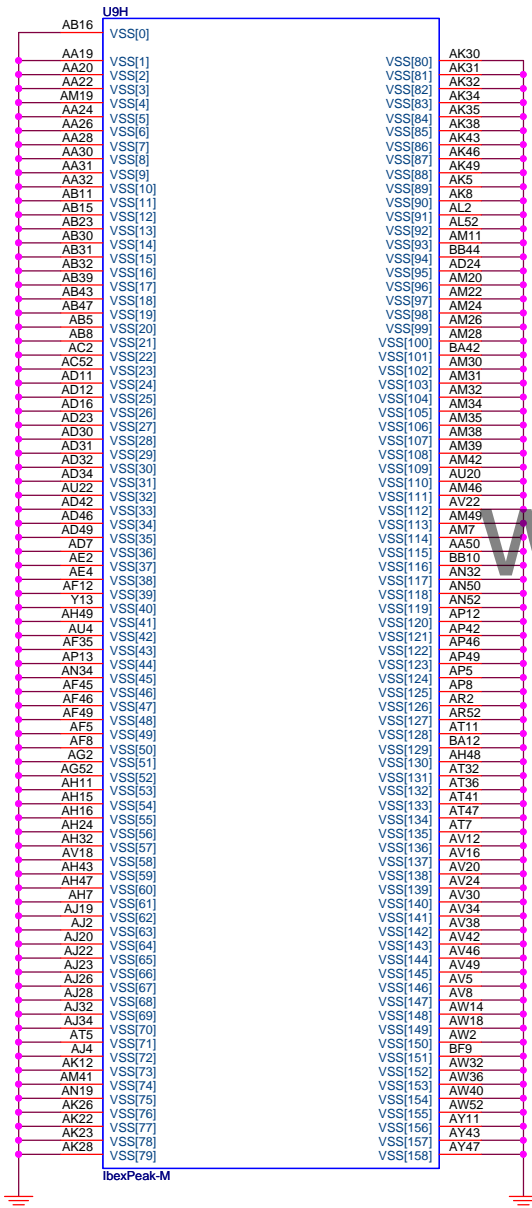
1UF*2 pcs for 2 blocks

Internal VRM supply

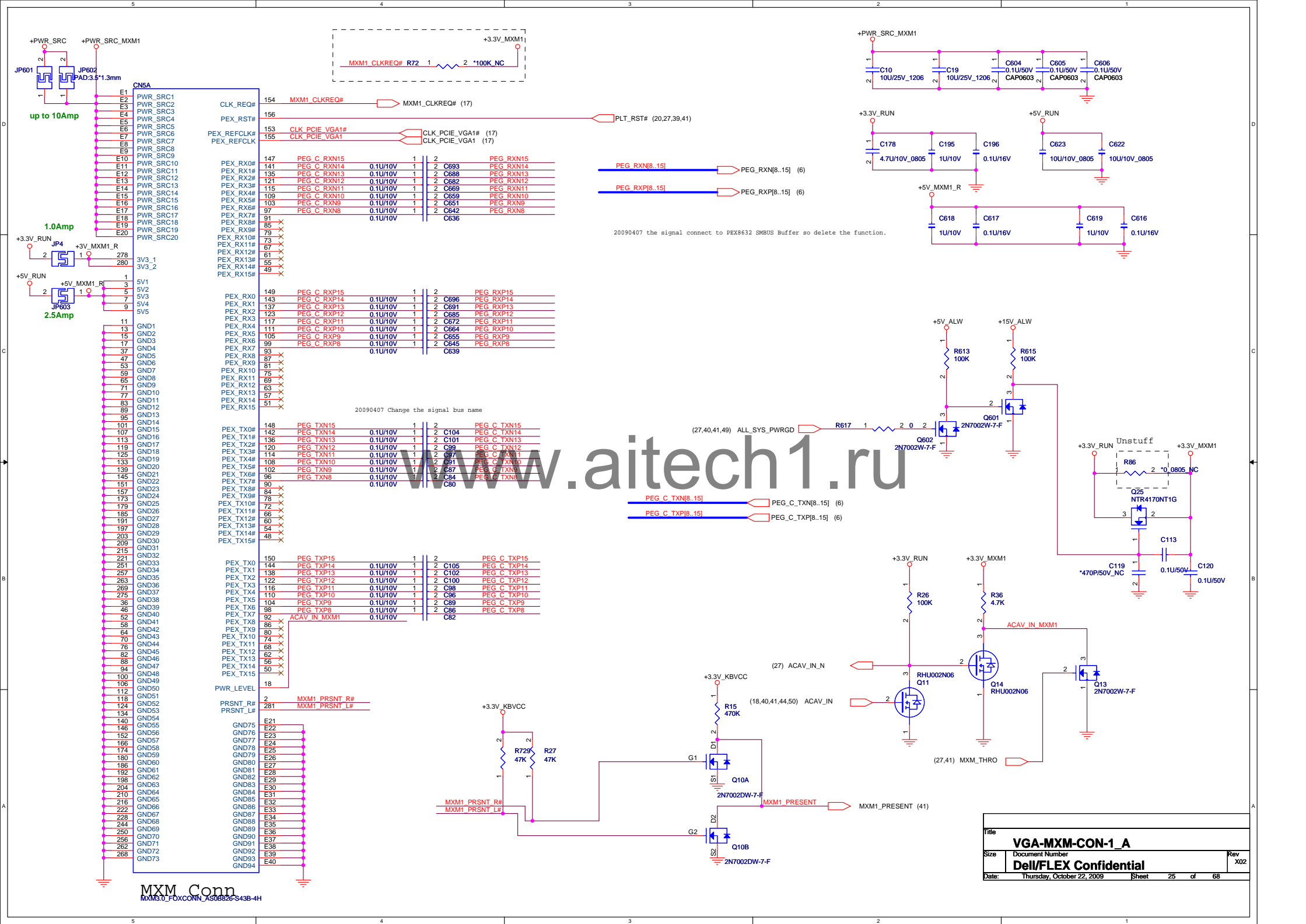
Internal VRM supply

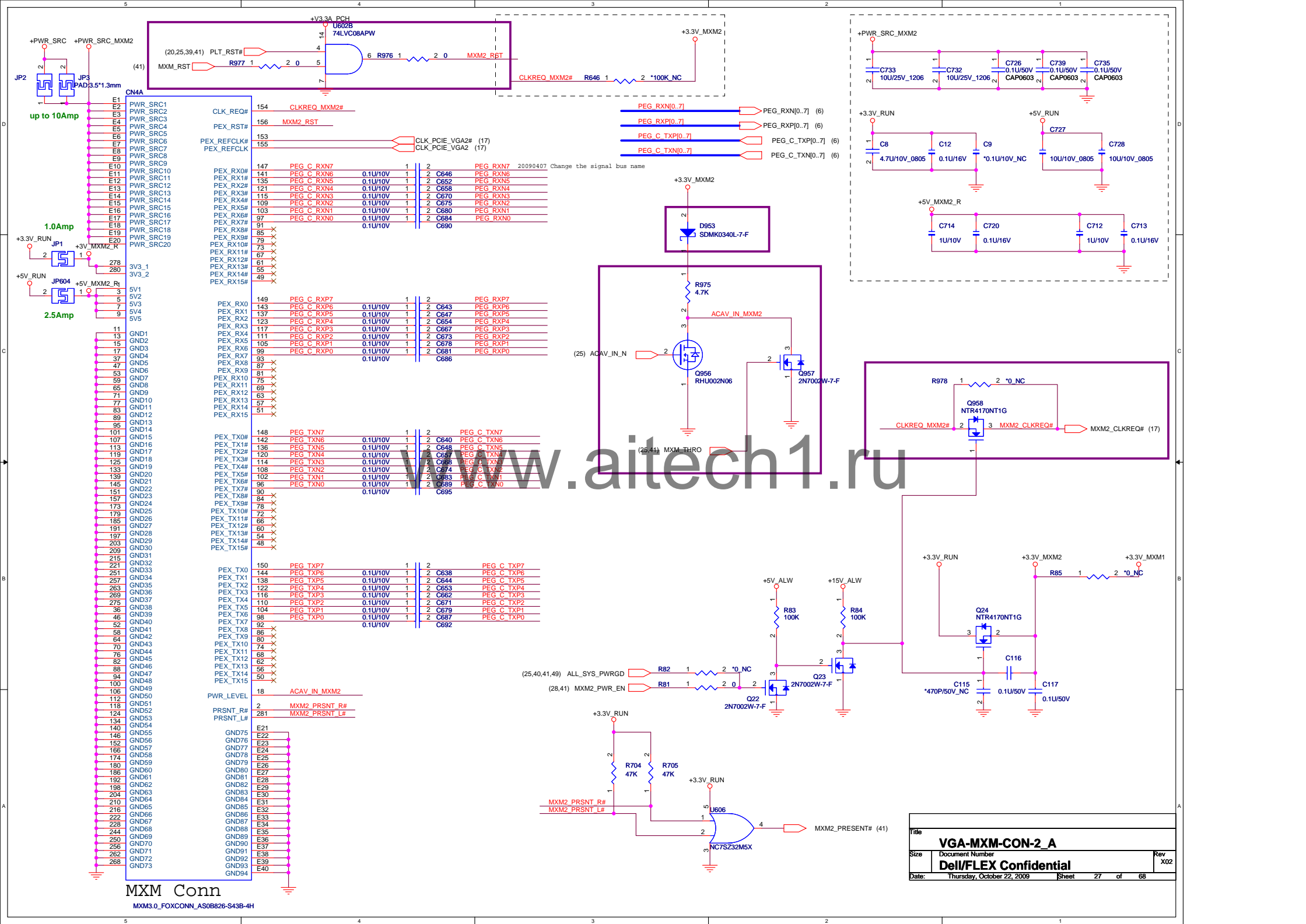
Title			PCH(POWER2) 8/9		
Size			Document Number		
			Dell/FLEX Confidential		
Date:			Thursday, October 22, 2009		
Sheet			23 of 68		
			Rev X02		

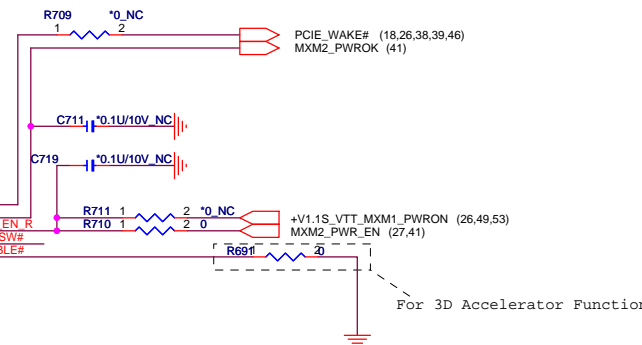
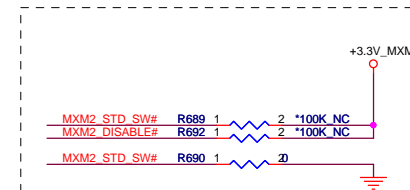
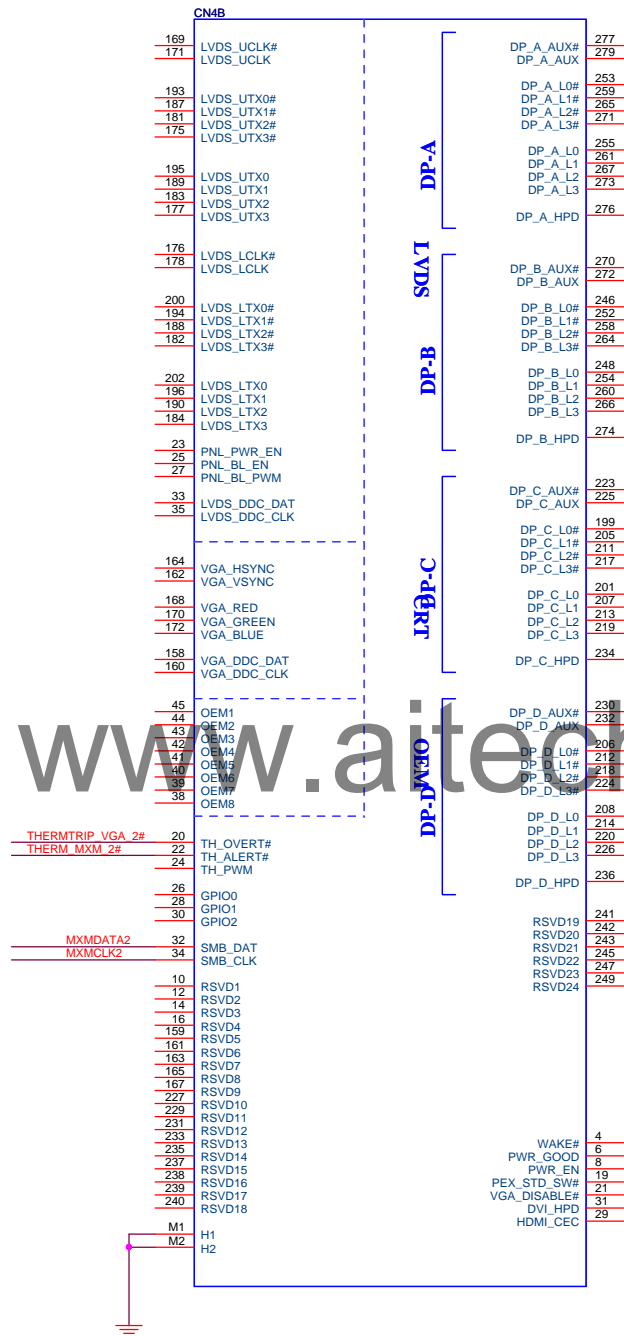
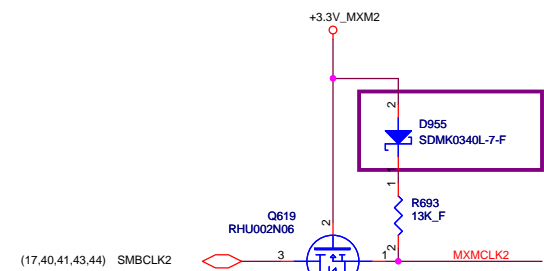
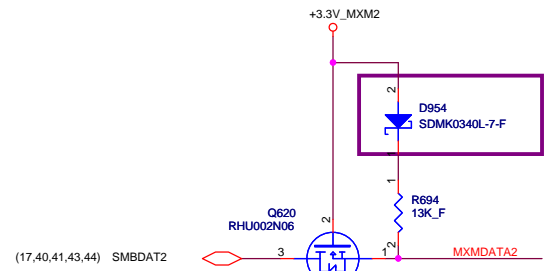
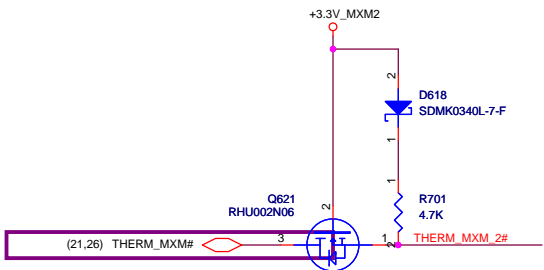
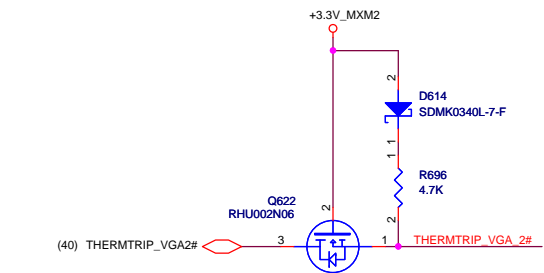
IBEX PEAK-M (GND)



Title		
PCH(GND) 9/9		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
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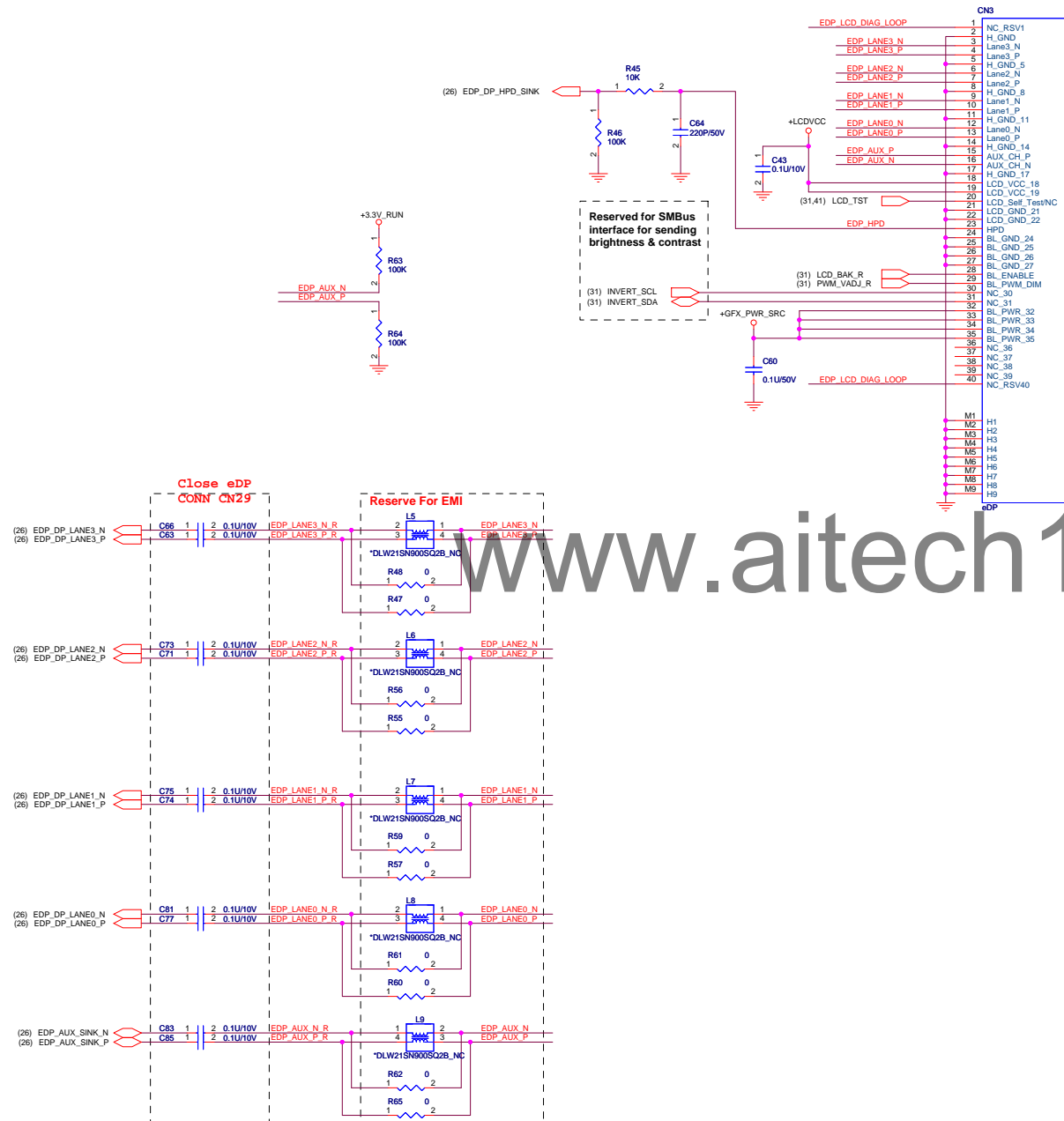


MXM Conn

MXM3.0_FOXCONN_AS0826-S43B-4H

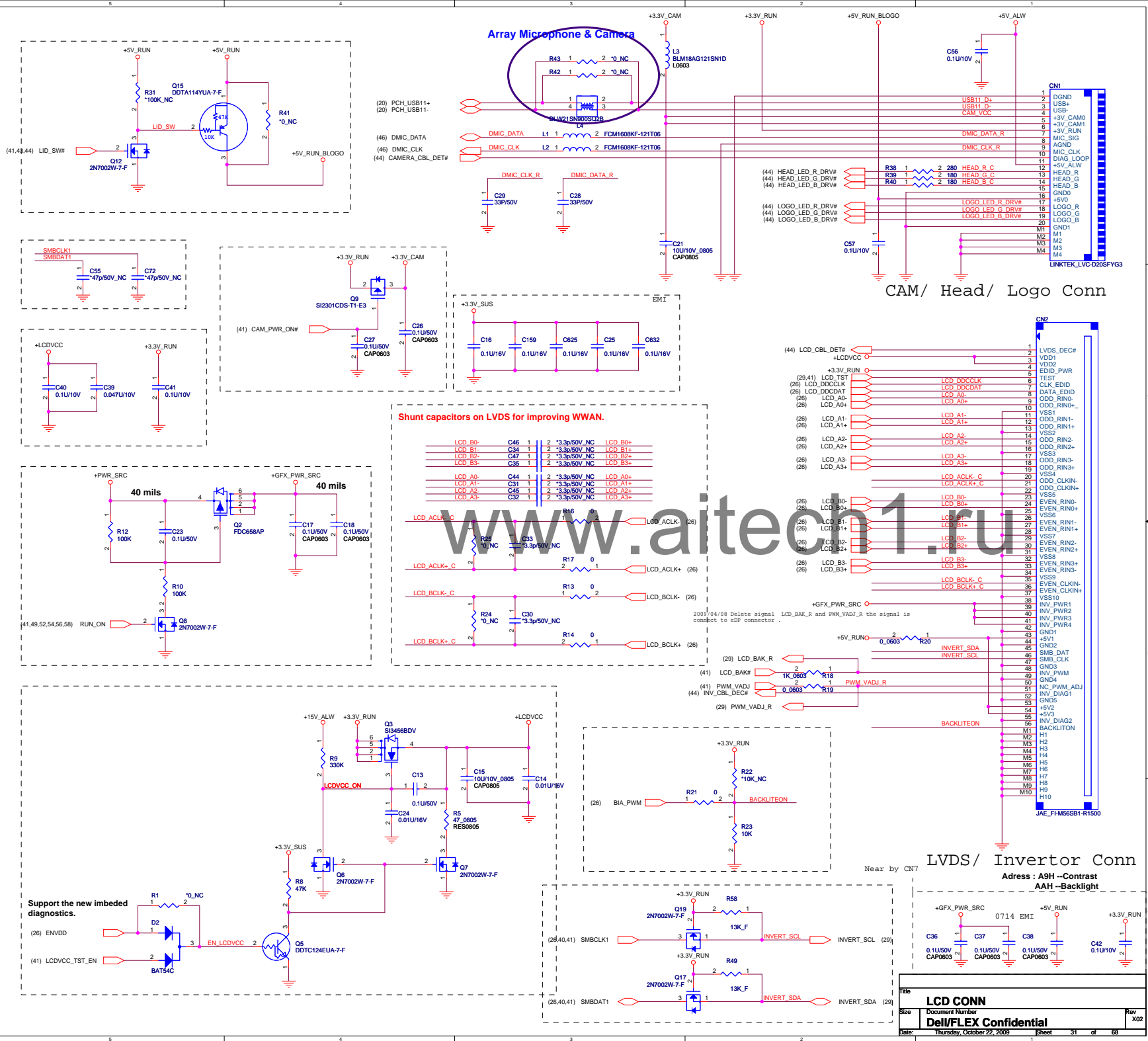
Title		
VGA-MXM-CON-2_B		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
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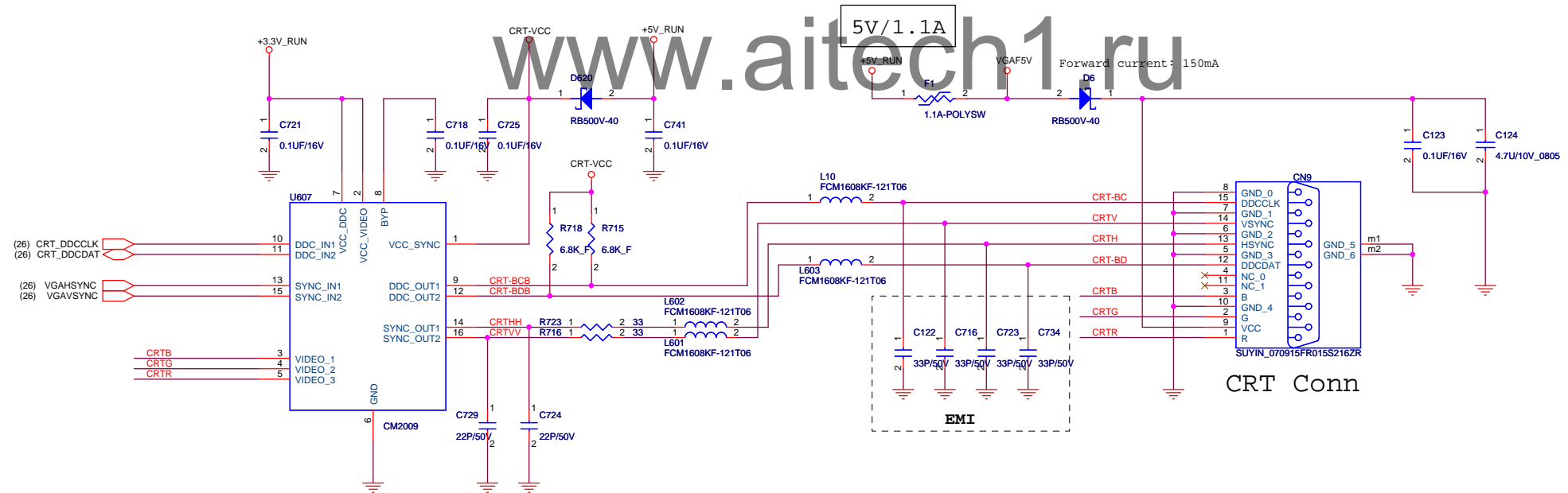
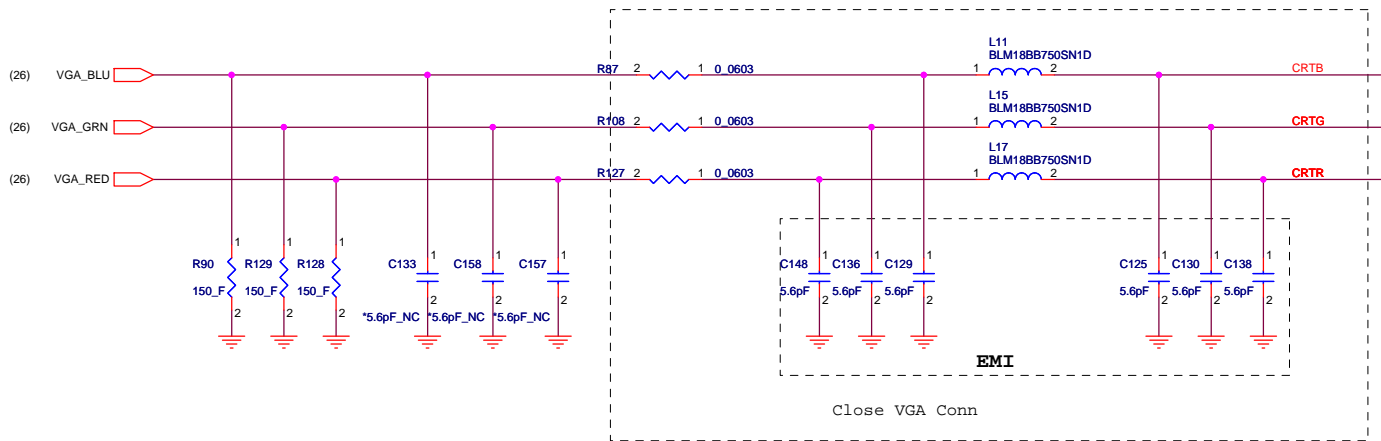
Embedded DISPLAY PORT CONNECTOR



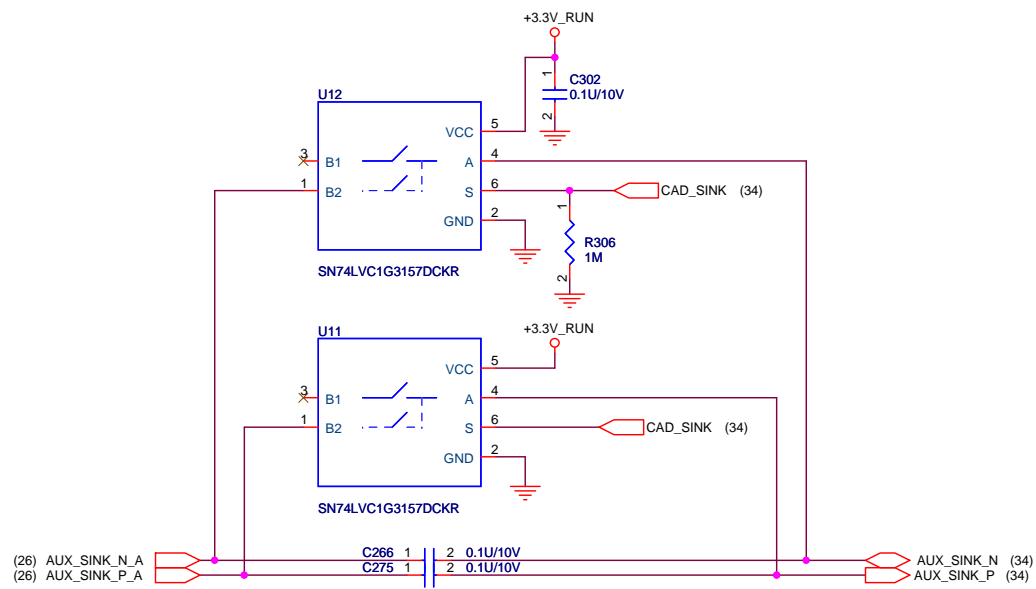
www.aitech1.ru

Title		
HDMI SELECTION		
Size	Document Number	Rev
	Dell/FLEX Confidential	X02
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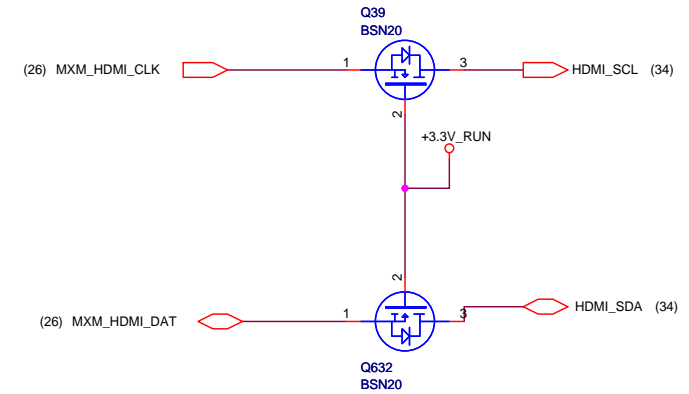




Title		
CRT CONN		
Size	Document Number	Rev
	Del/FLEX Confidential	X02
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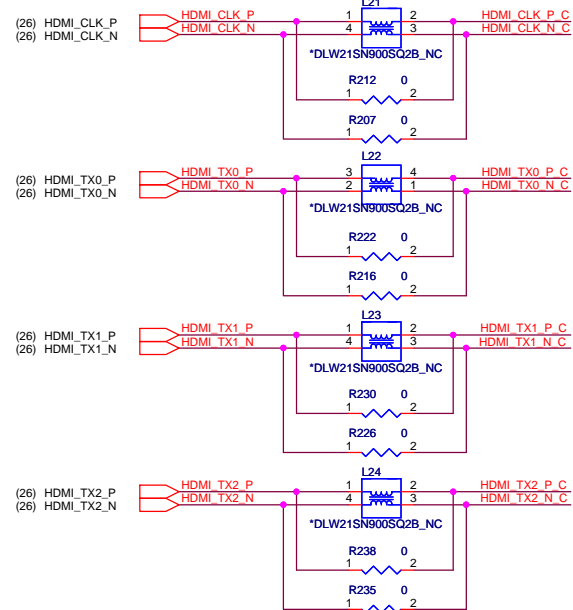
CAD_SINK	SOURCE
L	A=B1 (AC couple)
H	A=B2 (DDC)



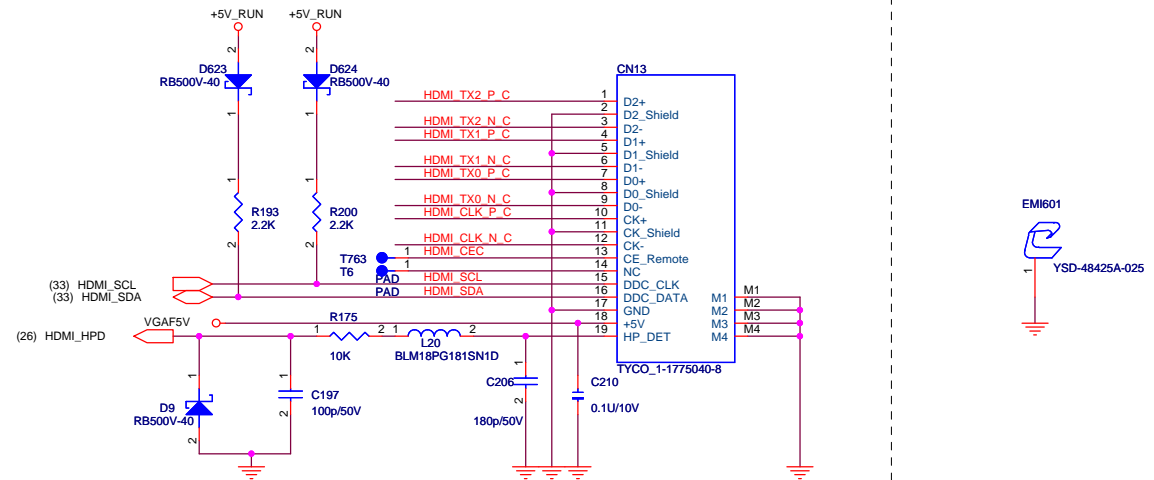
www.aitech1.ru

Title			
PCH DDC/ AUX MUX			
Size	Document Number		Rev
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Reserve For EMI

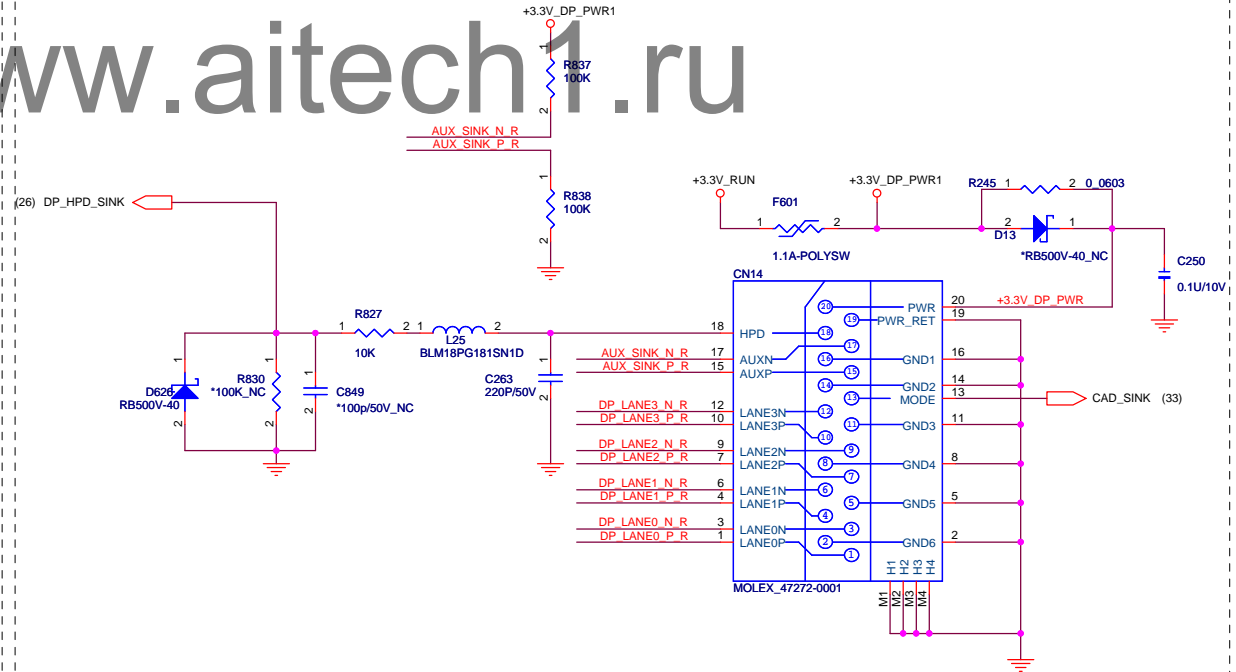
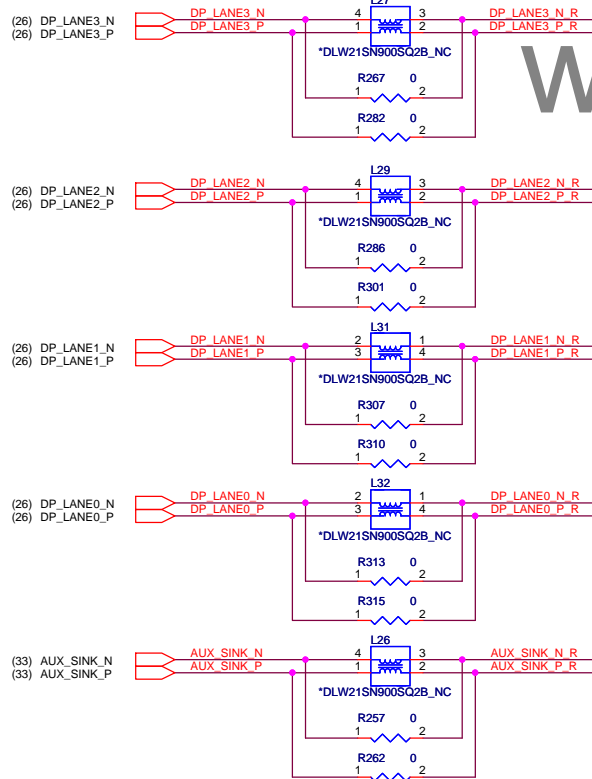


HDMI CONNECTOR

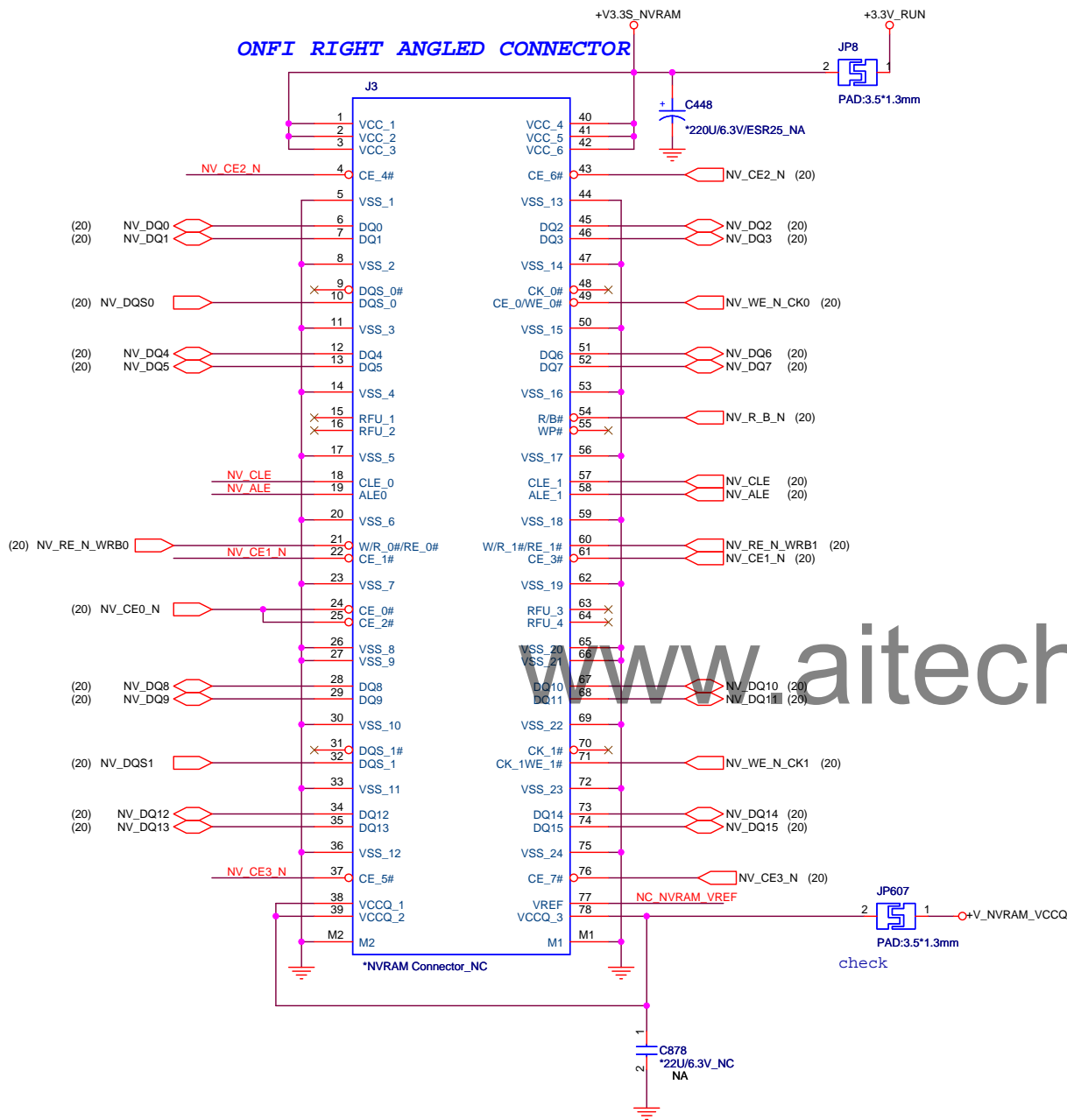


DISPLAY PORT CONNECTOR

Reserve For EMI



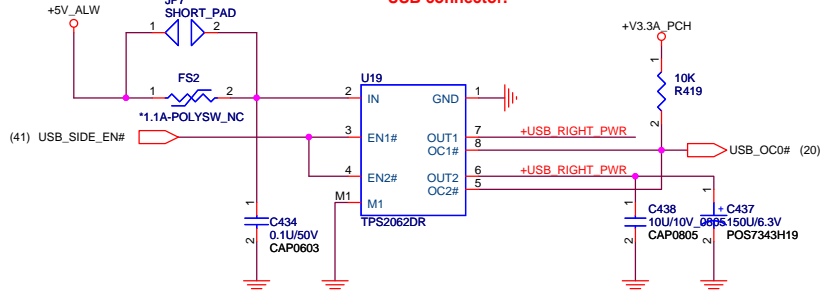
Title			HDMI & DP CONN
Size	Document Number	Rev	
	Del/FLEX Confidential	X02	
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Title		
ONFI Connector		
Size	Document Number	Rev
	Dell/FLEX Confidential	X02
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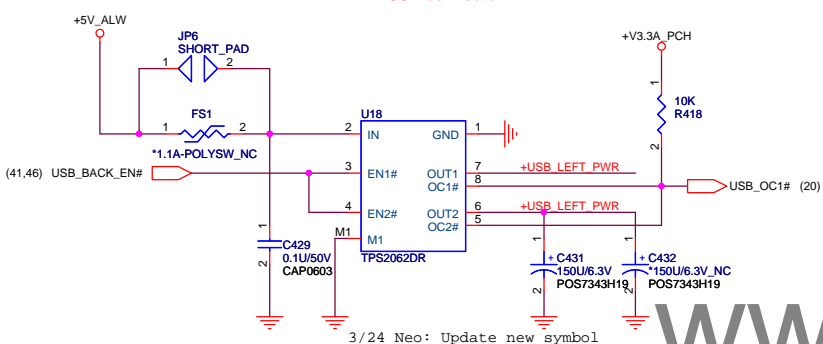
USB POWER SW

Place one 150uF cap by each USB connector.
Each channel is 1A



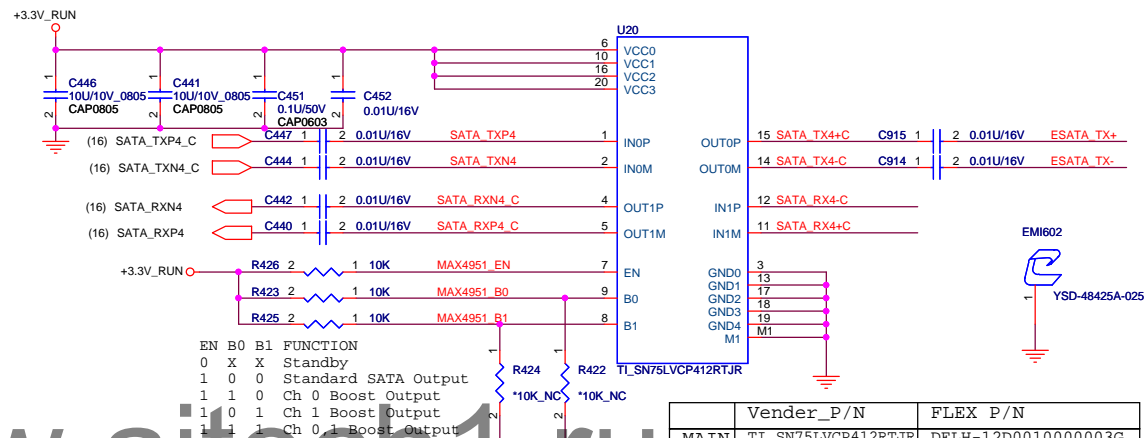
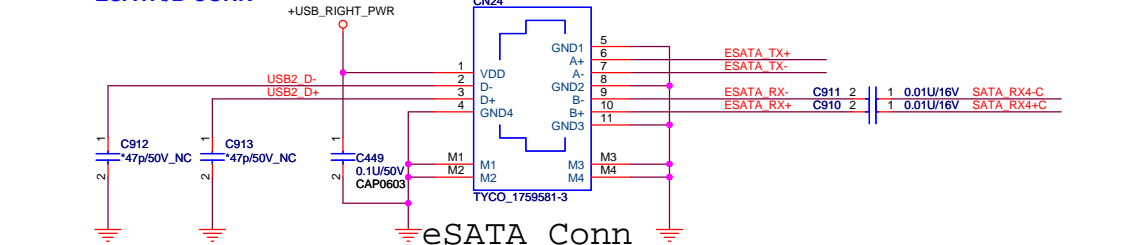
USB POWER SW

Place one 150uF cap by each USB connector.
Each channel is 1A



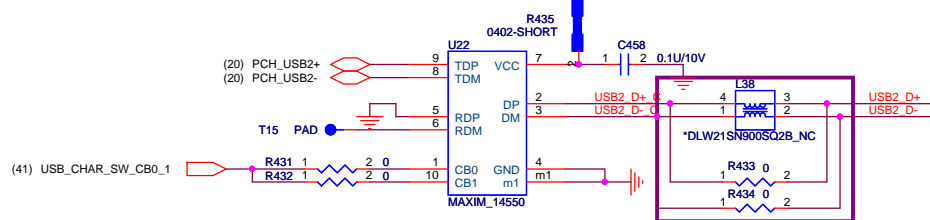
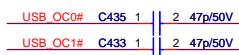
3/24 Neo: Update new symbol

ESATA/B CONN

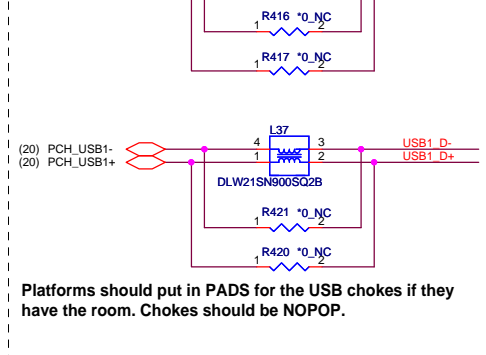


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0.1 Boost Output

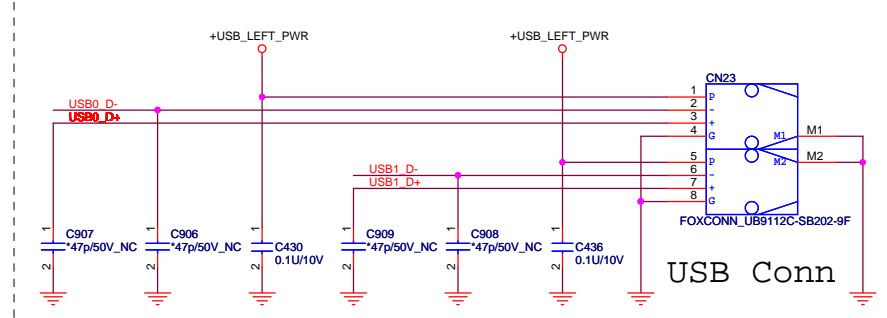
	Vender_P/N	FLEX P/N
MAIN	TI_SN75LVCP412RTJR	DELH-12D0010000003G
2ND	MAXIM_MAX4951	DELH-12D0010000001G



USB CONN

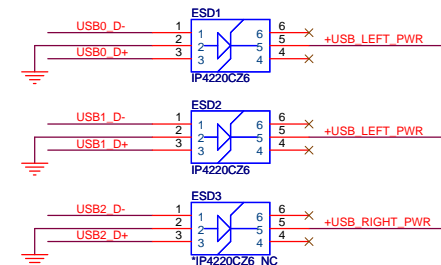


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



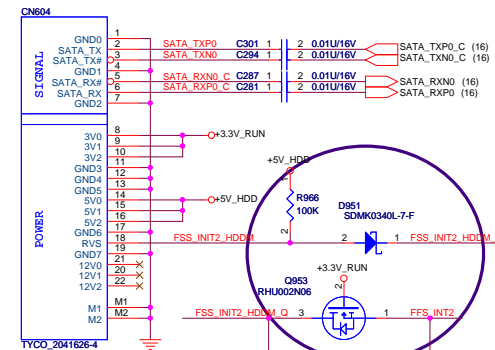
USB Conn

Place ESD diodes as close as USB connector.

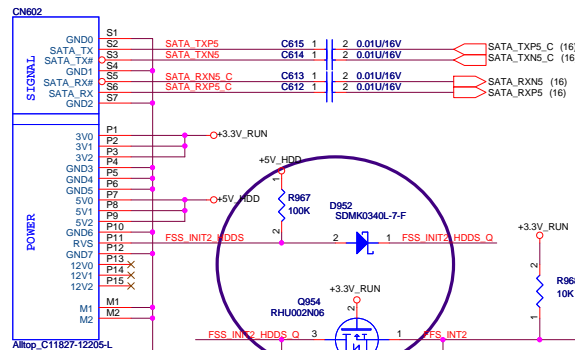


Title		
USBx2 & eSATA		
Size	Document Number	Rev
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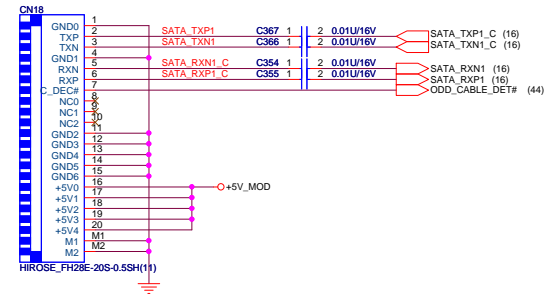
SATA Connector Master HDD Conn



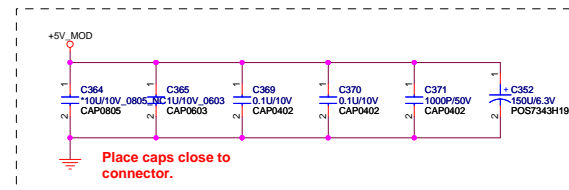
Slave HDD Conn



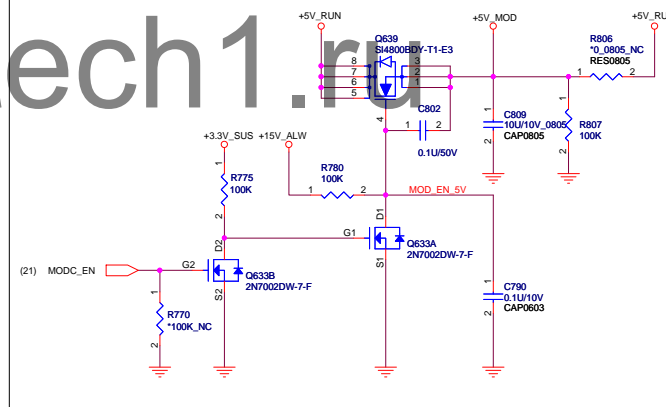
ODD Connector



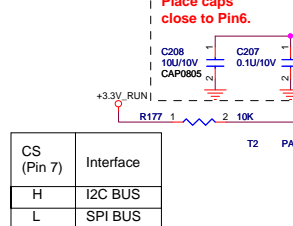
ODD Conn



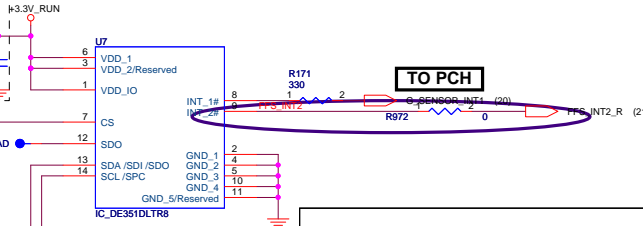
www.aitech1.ru



G-Sensor

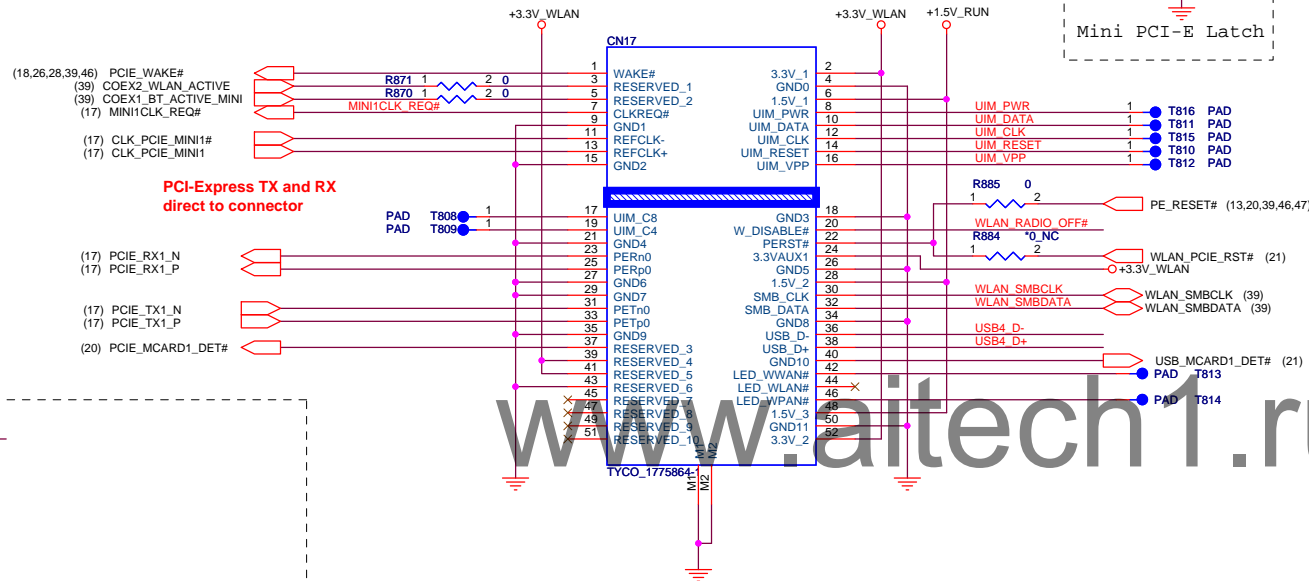


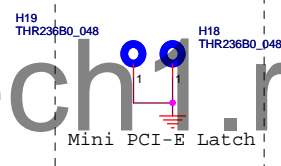
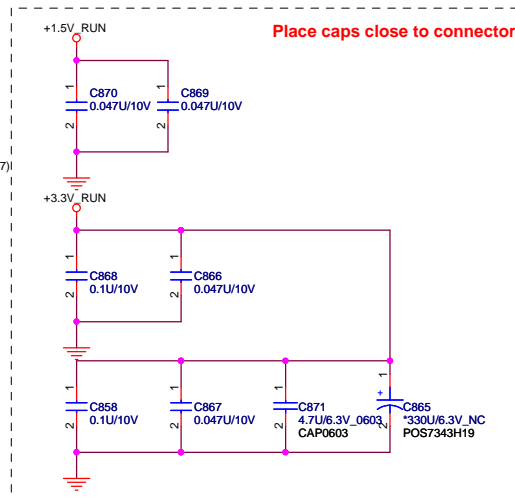
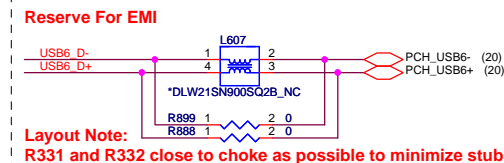
CS (Pin 7)	Interface
H	I2C BUS
L	SPI BUS

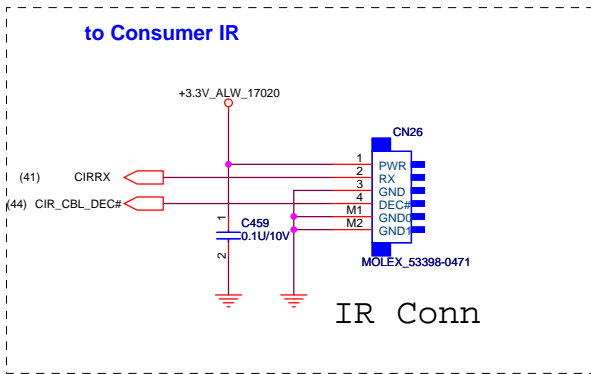
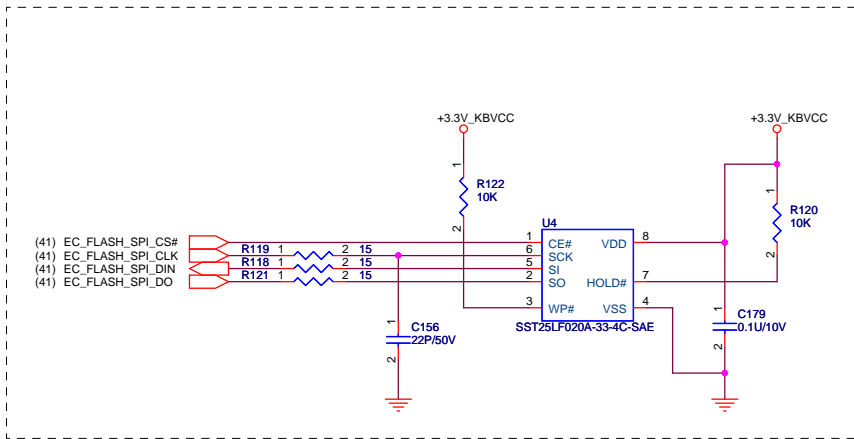


File	HDDx2 & CD ROM
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MiniCard WMAX Connector

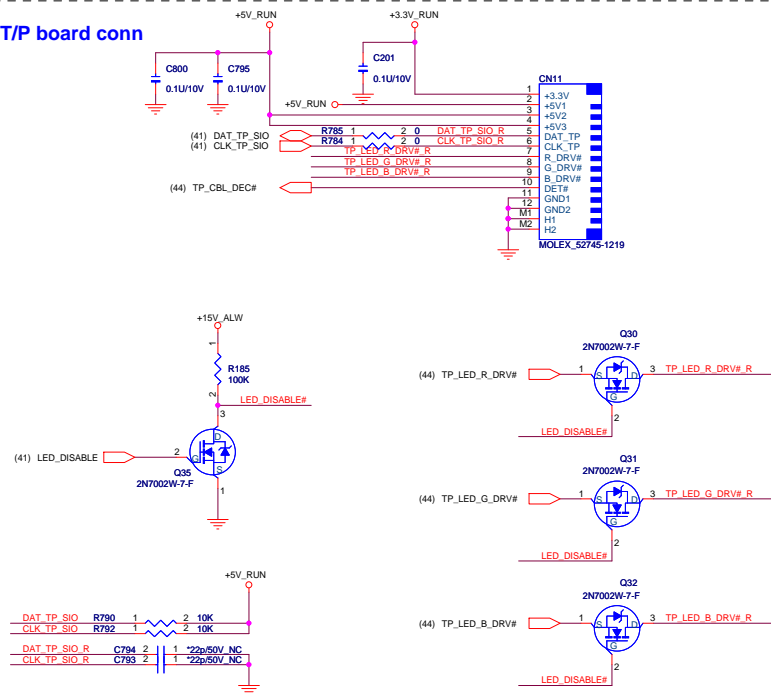




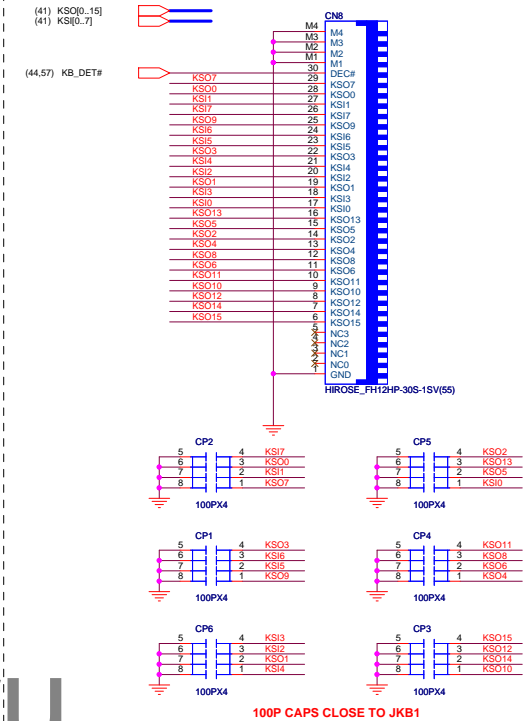


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T/P board conn

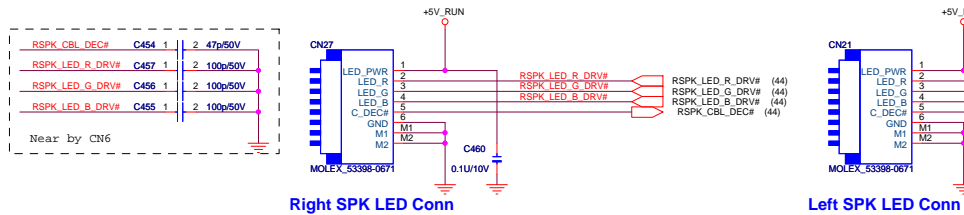


KEYBOARD CONNECTOR

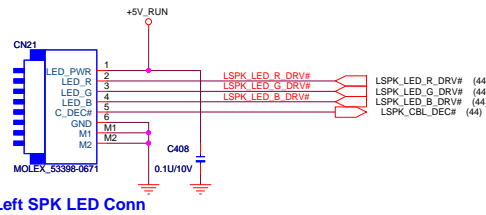


www.aitech1.ru

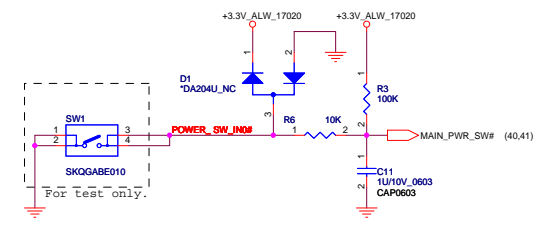
Right SPK LED Conn



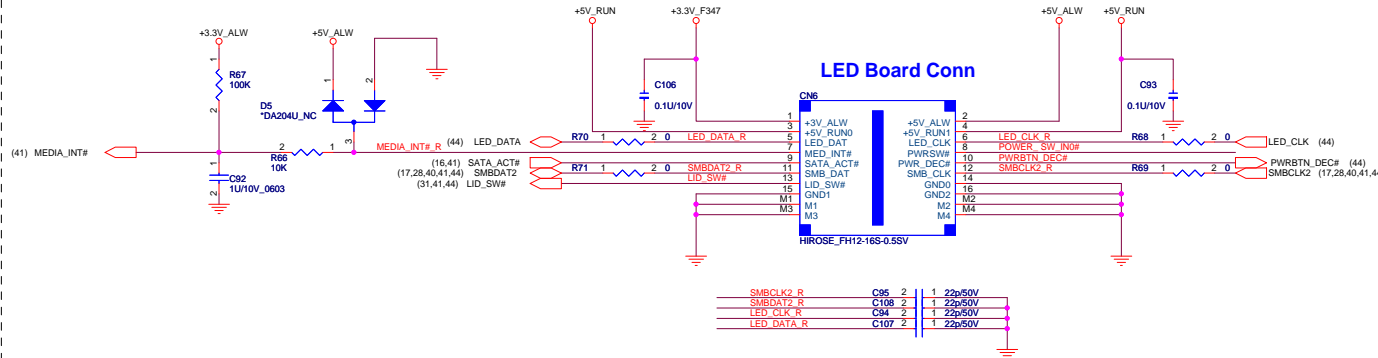
Left SPK LED Conn

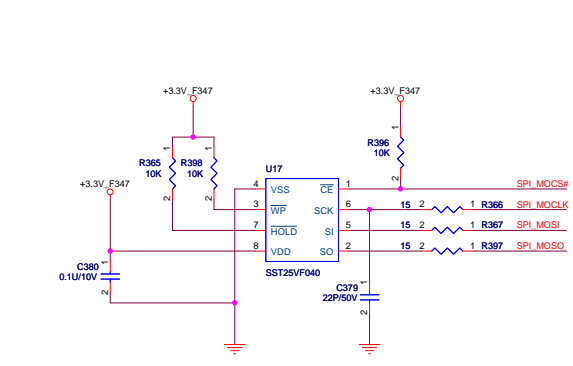
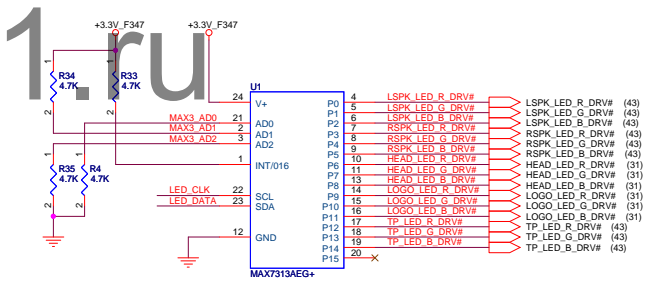
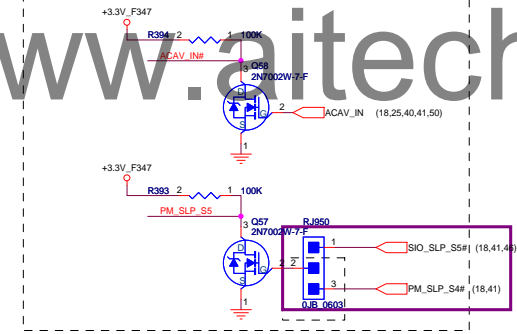
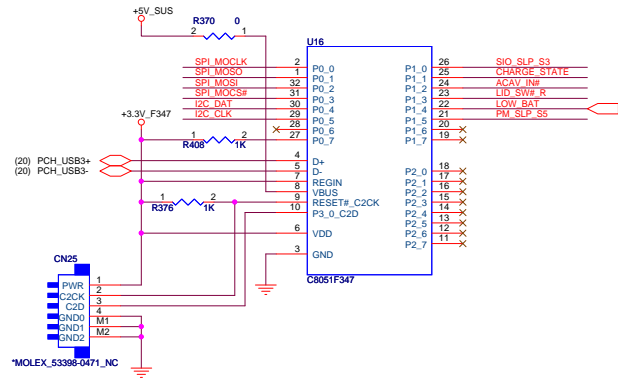
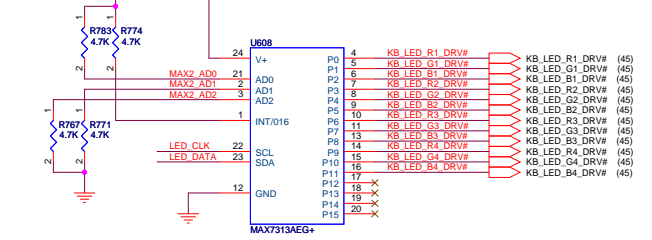
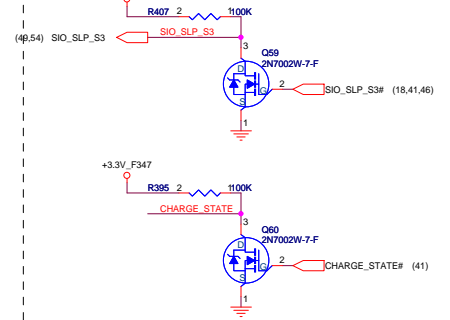
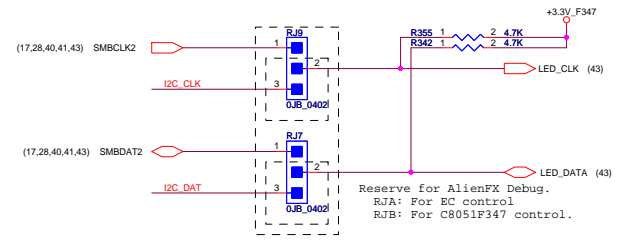
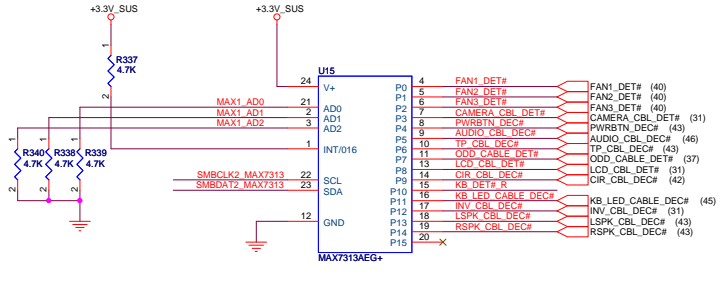
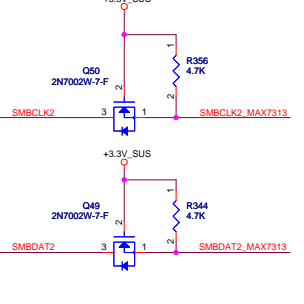
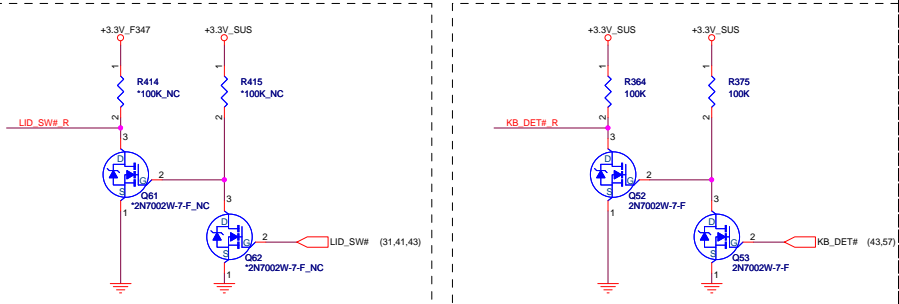


Power Button



LED Board Conn

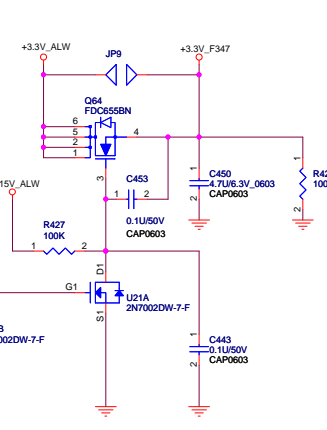




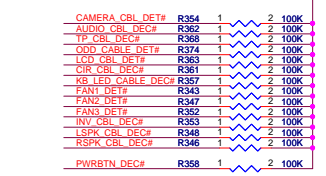
+3.3V_F347 behavior

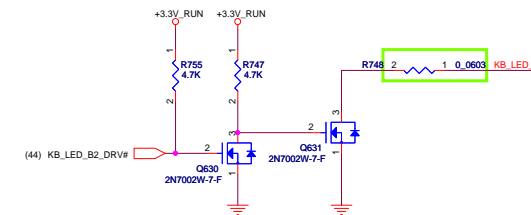
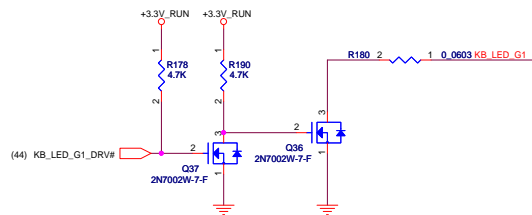
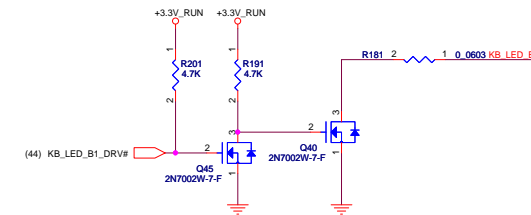
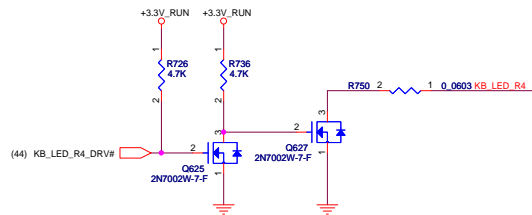
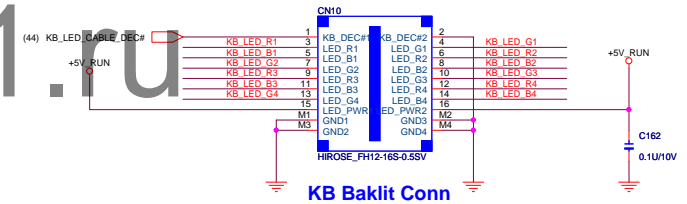
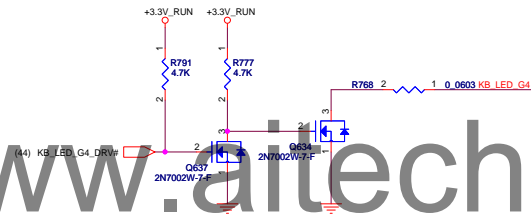
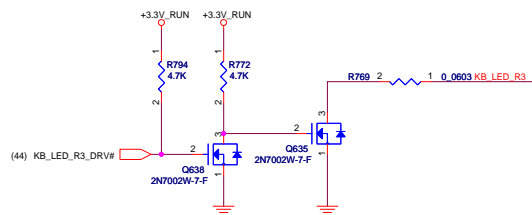
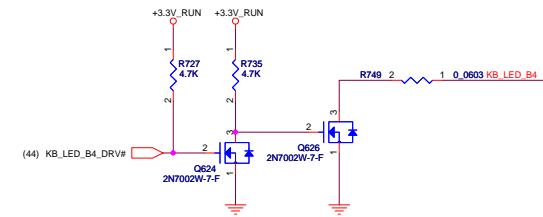
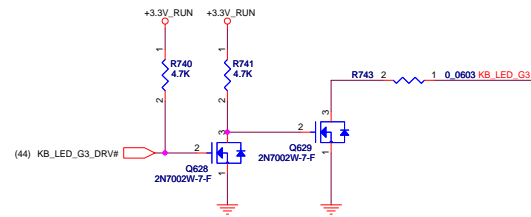
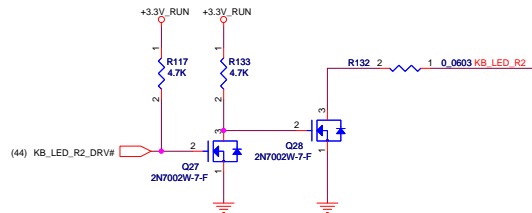
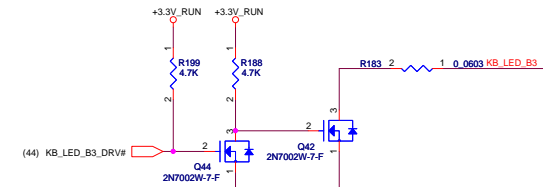
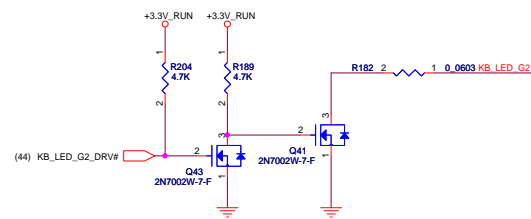
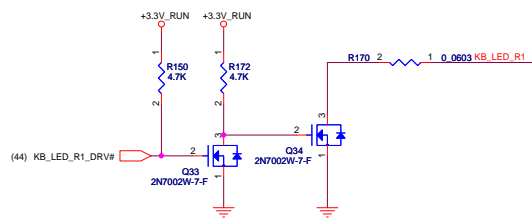
	State				
	S0	S3	S4	S5	
AC In	ON	ON	ON	ON	
BAT only	ON	ON	Off	Off	

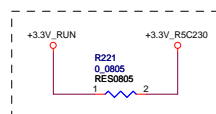
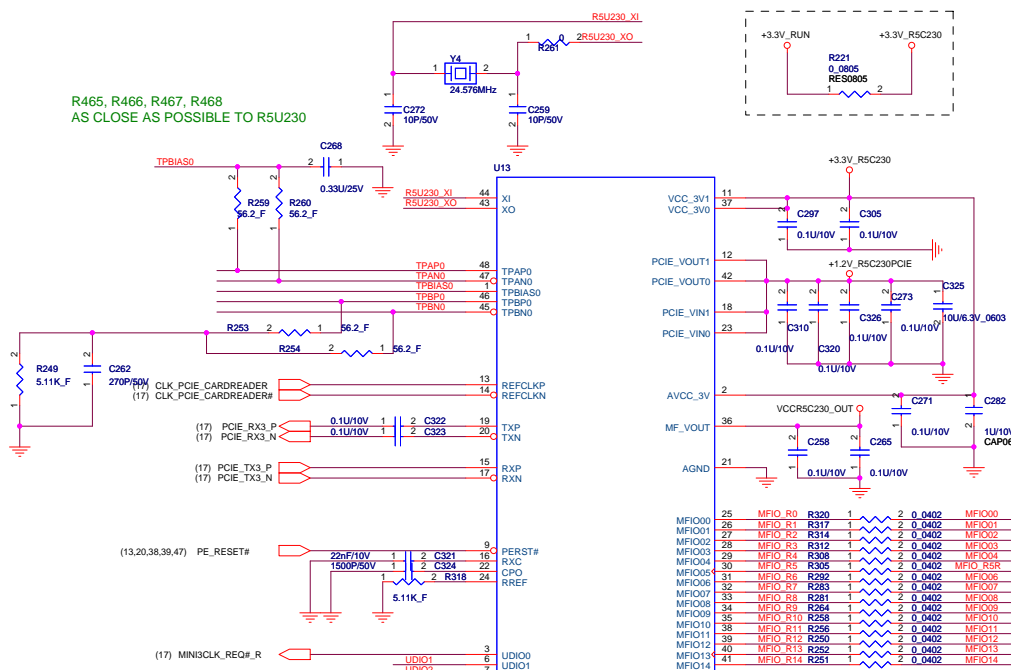
AC mode Battery full in S5:
turn off ELC controller.



Reference	AD2	AD1	AD0	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPK& Head& Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

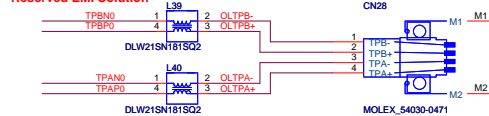
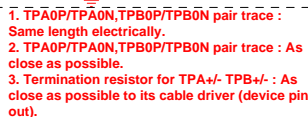
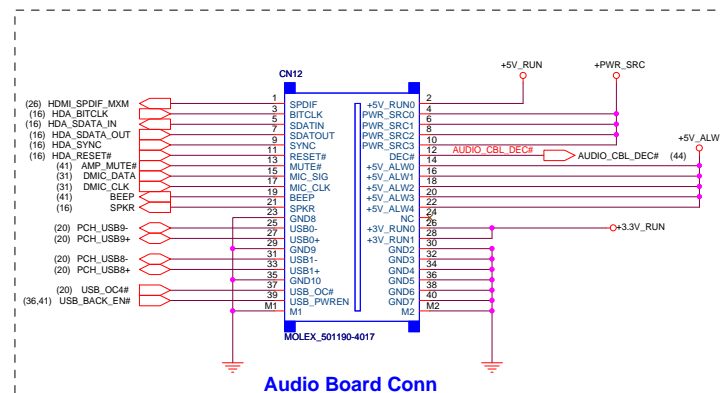








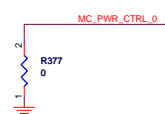
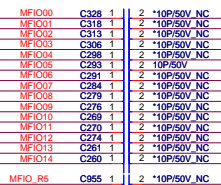
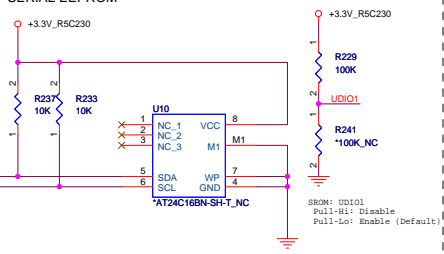
MFIO Pin Assignment Table

	MFIO	SD8	XD	MS8
00	WP	D7	BS	
01	D1	D6	-	
02	D0	D5	D1	
03	D7	D4	-	
04	D6	D3	D5	
05	CLK	D2	D0	
06	-	D1	-	
07	D5	D0	D2	
08	CMD	WP#	D4	
09	D4	WE#	D6	
10	D3	ALE	D3	
11	D2	CLE	-	
12	-	CE#	-	
13	-	RE#	D7	
14	-	R/B#	CLK	
MFCD0#	CD#	CD0#		
MCN0#	-	CD1#	INS#	

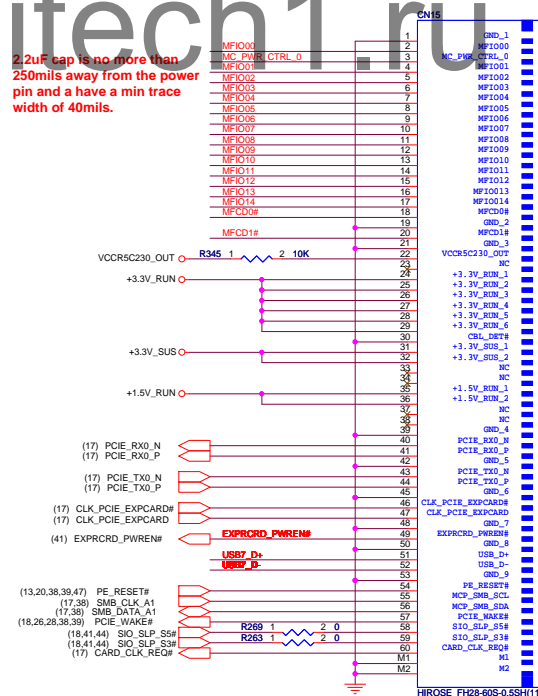


1394 Conn

TPBN0	R437	1		2	*0 NC	OLTPB-
TPBP0	R436	1		2	*0 NC	OLTPB+
TPAN0	R439	1		2	*0 NC	OLTPA-
TPAP0	R438	1		2	*0 NC	OLTPA+

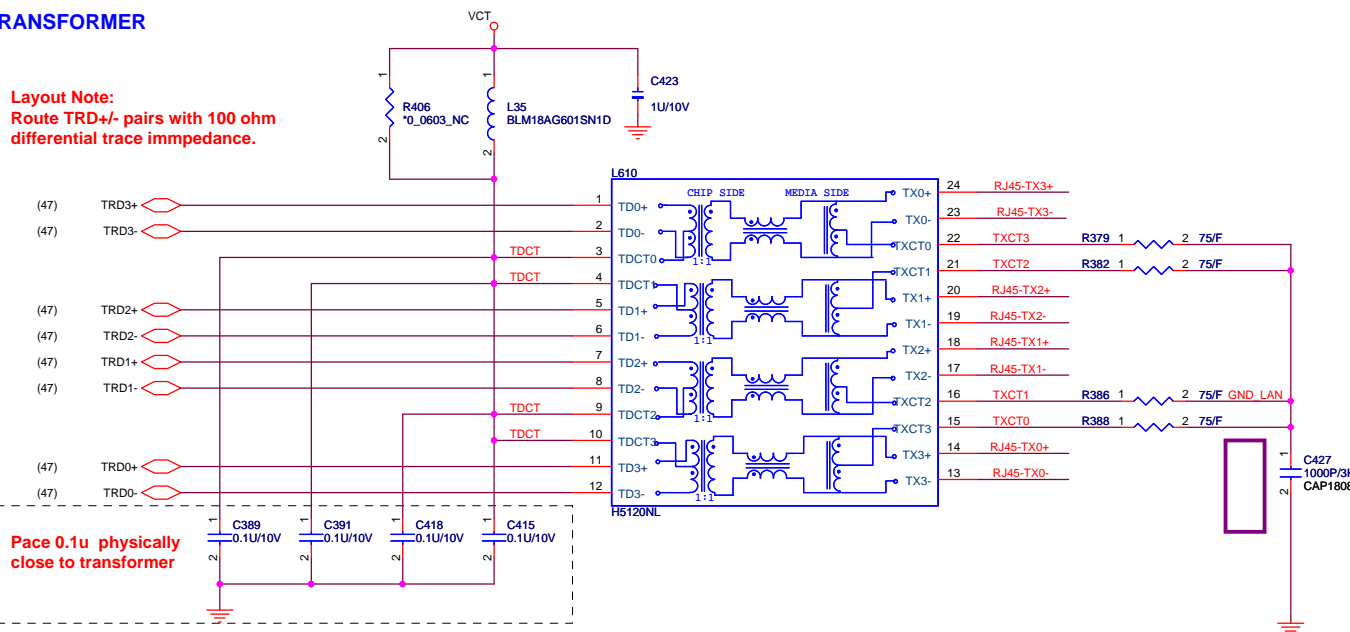


Express Card Conn

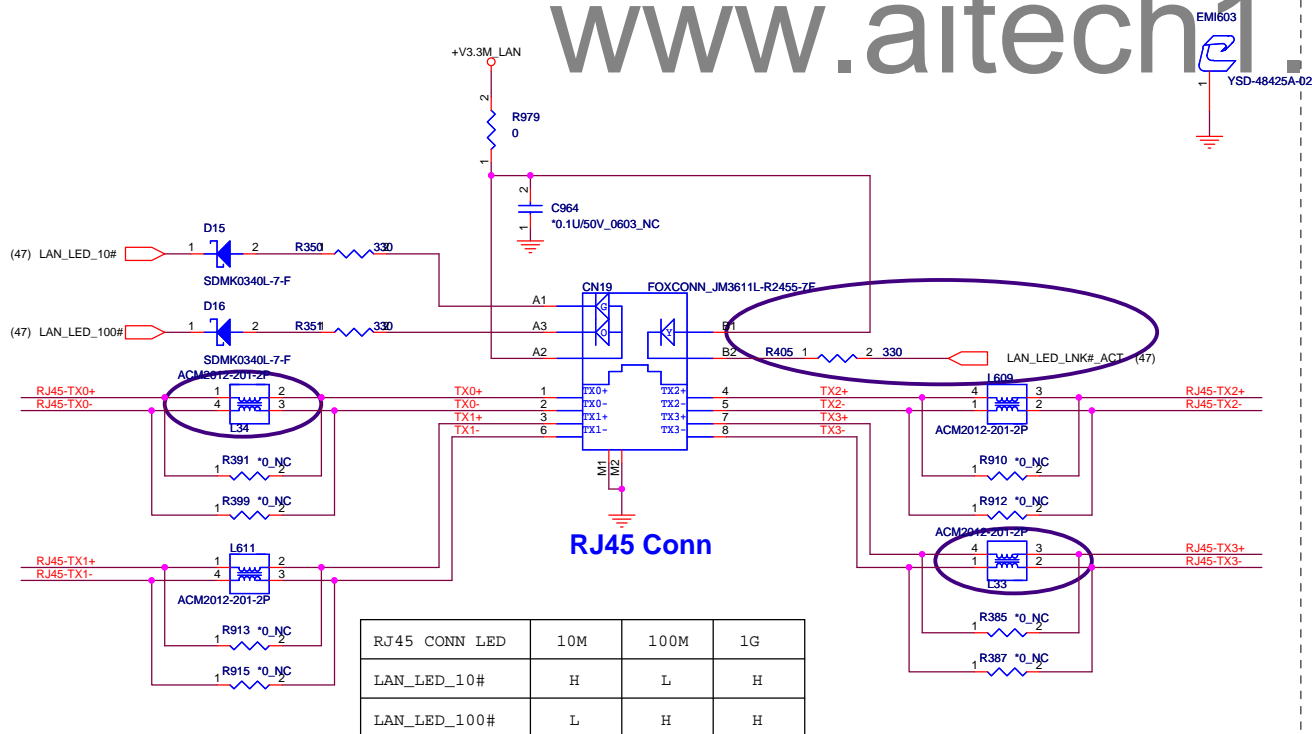


TRANSFORMER

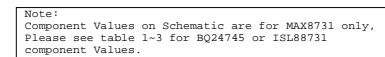
Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



RJ-45 Connector



RJ45 CONN LED	10M	100M	1G
LAN_LED_10#	H	L	H
LAN_LED_100#	L	H	H



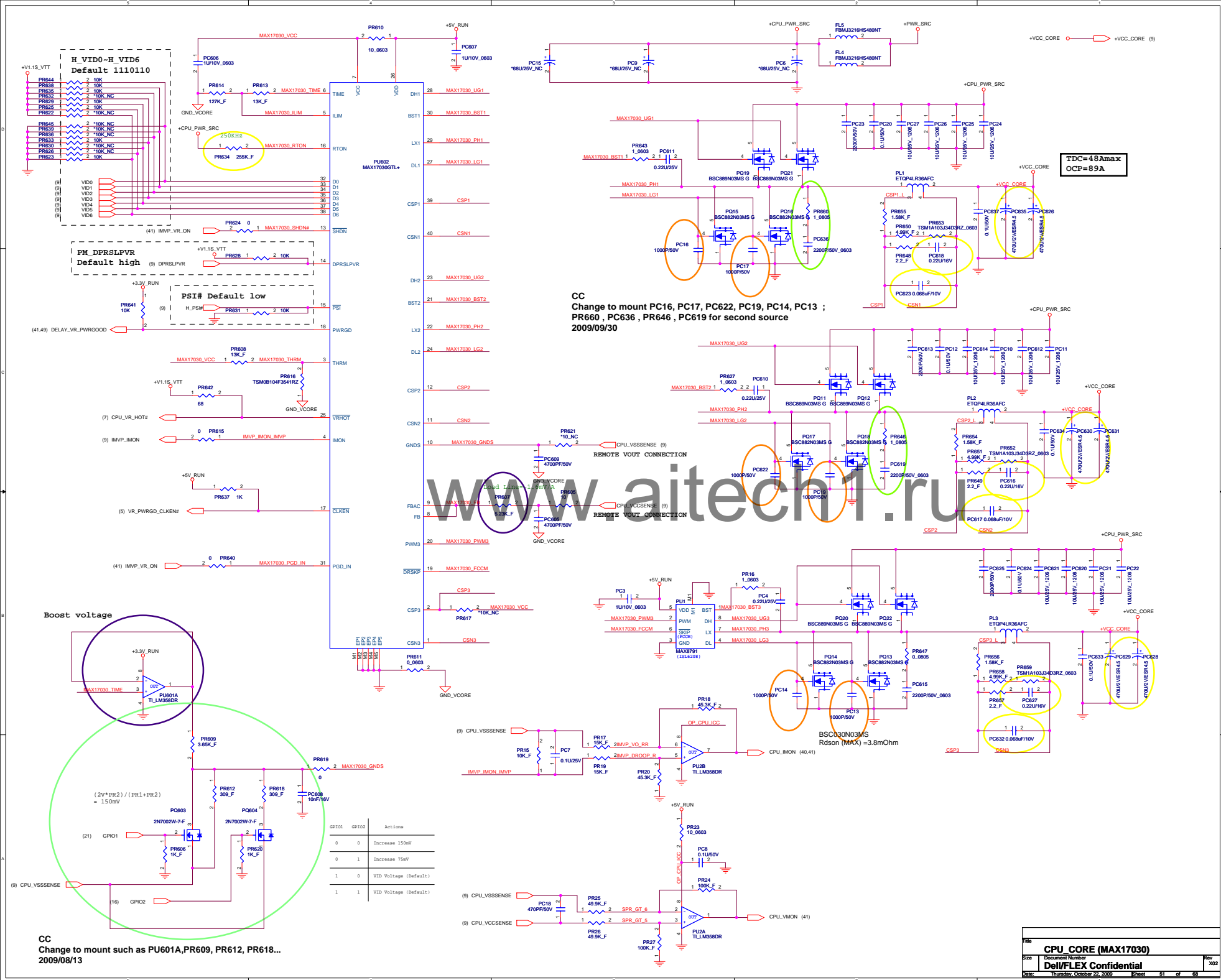
PIN	MAX8731A	ISL8731	bq24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMF	PFE
7	DIAC	NC	DI
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LAGE	LAGE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGATE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

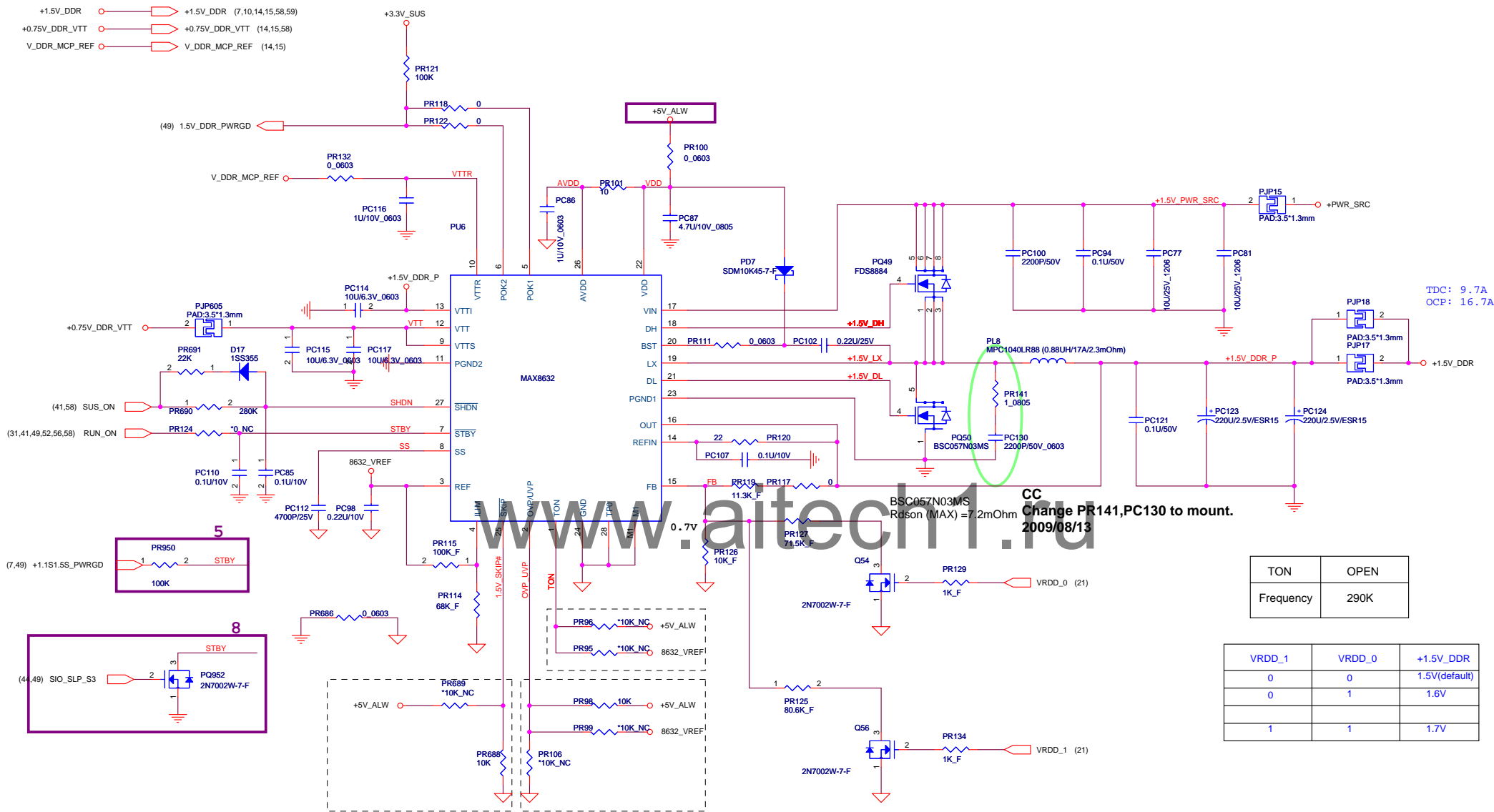
*NC = means no connect

REF DES	MAXIM	INTERSI	TI
PR245	NO STUFF	10K, 0402, 5%	NO STUFF
PC227	0 0402, 5%	10, 0402, 5%	0 0402, 5%
PR228	0 0402, 5%	10 0402, 5%	0 0402, 5%
PC157	NO STUFF	0 1uF	0 1uF
PC202	NO STUFF	NO STUFF	0 1uF
PC203	NO STUFF	NO STUFF	NO STUFF
PR230	0 0402, 5%	10 0402, 5%	0 0402, 5%
PR231	0 0402, 5%	10 0402, 5%	0 0402, 5%
PC207	NO STUFF	NO STUFF	0 1uF
PC208	NO STUFF	0 1uF	0 1uF
PC209	NO STUFF	NO STUFF	NO STUFF
PR17	8.2K, 0402, 5%	2.2K, 0402, 5%	4.7K, 0402, 5%
PR18	8.45K, 0402, 5%	NO STUFF	NO STUFF
PR232	NO STUFF	NO STUFF	200K, 0402, 5%
PC233	NO STUFF	NO STUFF	75K, 0402, 5%
PR234	NO STUFF	NO STUFF	9 0402, 5%
PC23	0.1uF, 0402, 10V	NO STUFF	200pF, 0402, 10V
PC24	0.01uF	0.01uF	NO STUFF
PC210	NO STUFF	NO STUFF	130pF, 0402, 10V
PC211	0.01uF	NO STUFF	NO STUFF
PC153	0.01uF	0.01uF	NO STUFF
PC204	NO STUFF	NO STUFF	51pF, 0402, 10V
PC206	NO STUFF	NO STUFF	2000pF, 0402, 10V
PC27	1.0uF, 0603, 10V	NO STUFF	1.0uF, 0603, 10V
PC28	0.1uF, 0402, 10V	NO STUFF	NO STUFF
PR10	10K, 0402, 1%	10K, 0402, 1%	NO STUFF
PR17	15.8K, 0402, 1%	15.8K, 0402, 1%	NO STUFF
PR229	NO STUFF	NO STUFF	10K, 0402, 1%
PR5	355K, 0402, 1%	215K, 0402, 1%	305K, 0402, 1%
PC11	CH501H-40PT	NO STUFF	CH501H-40PT
PR6	33 0603, 1%	33 0603, 1%	NO STUFF
PC11	1.0uF, 0603, 10V	1.0uF, 0603, 10V	NO STUFF
PR12	1 0603, 1%	0 0603, 1%	0 0603, 1%
PR16	100 0402, 5%	100 0402, 5%	0 0402, 5%
PC22	220pF, 0402, 50V	NO STUFF	NO STUFF
PC29	0 0402, 5%	8.45K, 0402, 1%	8.45K, 0402, 1%
PC214	0.01uF	NO STUFF	NO STUFF
PR13	NO STUFF	NO STUFF	NO STUFF

TABLE 1								
			MAX8731A/SL88731			bg24745		
ADAPTER(W)	TRIP CURRENT (A)	R237	R241	R243	R242 (see Note 1)	R241	R243	R242 (see Note
65	3.17	57.6K	13K	105	24.9K	12.4K	205	24.3K
150	7.43	30.9K	24.9K	499	10.7K	23.7K	499	10.5K
240	(see Note 2) 11.69	17.8K	6.49K	3.48K	2.37K	8.45K	1.18K	23.2K

Note 1 : R242 is populated if ADAPT_TRIP_SET is used to program for the next lower adapter
ADAPT_TRIP_SET is floating for the higher adapter , grounded for the lower adapter
Note 2 : RR1 must be 5mOhms instead of 10mOhms for the 240W adapter





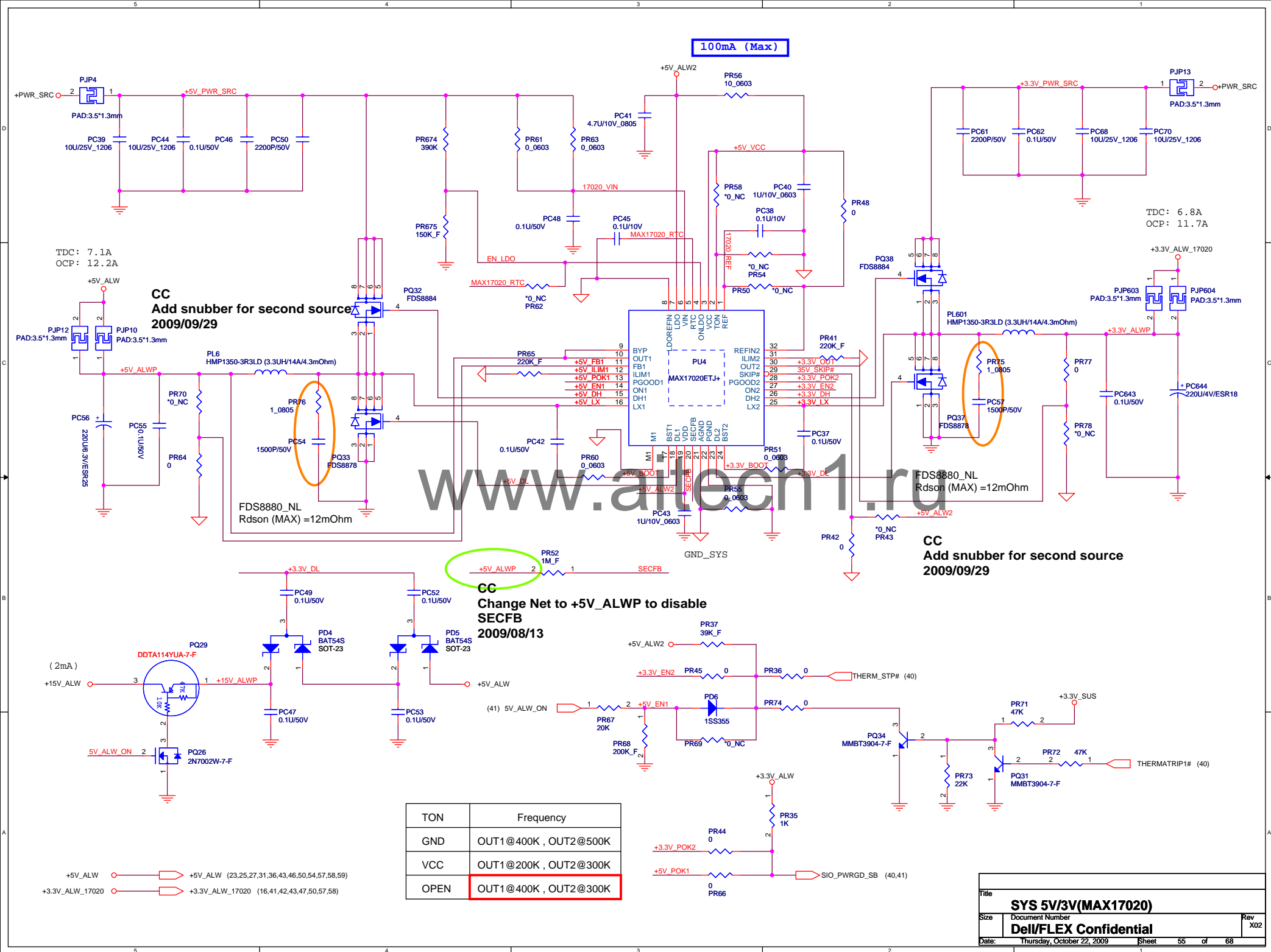
TDC: 9.7A
OCP: 16.7A

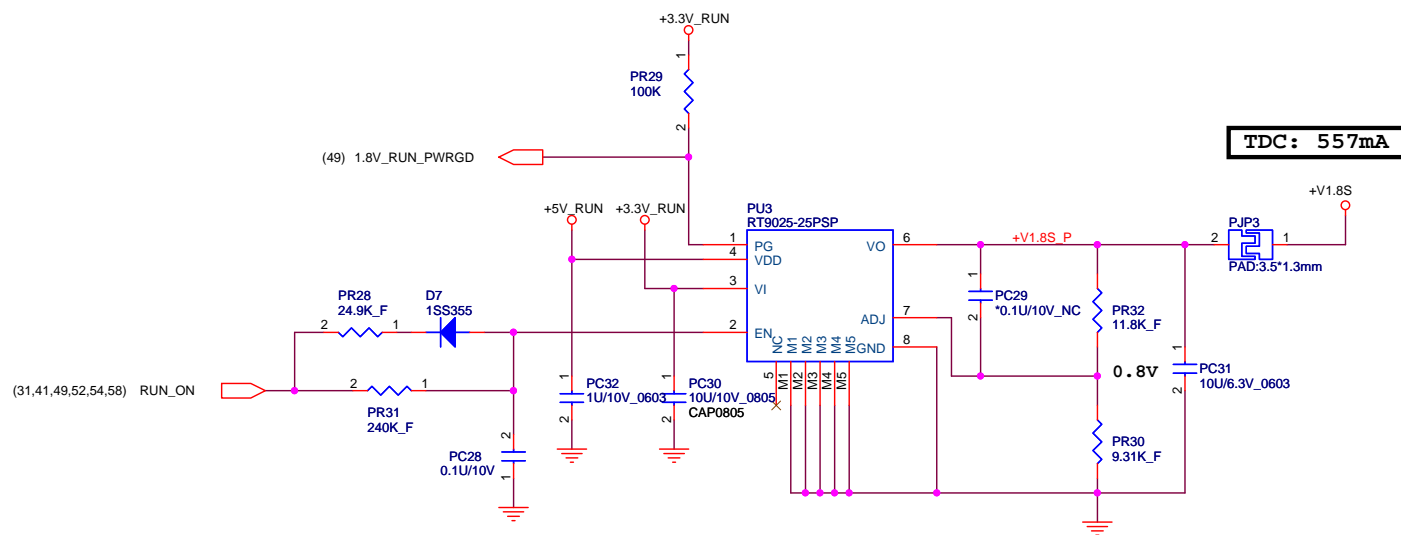
CC
Change PR141,PC130 to mount.
2009/08/13

TON	OPEN
Frequency	290K

VRDD_1	VRDD_0	+1.5V_DDR
0	0	1.5V(default)
0	1	1.6V
1	1	1.7V

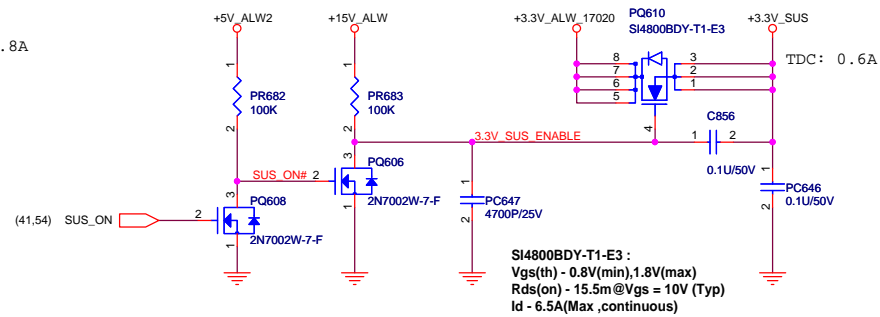
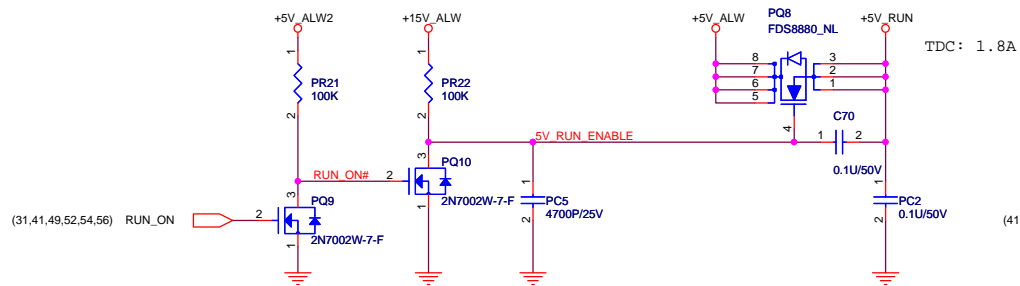
Title		
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Size	Document Number	Rev
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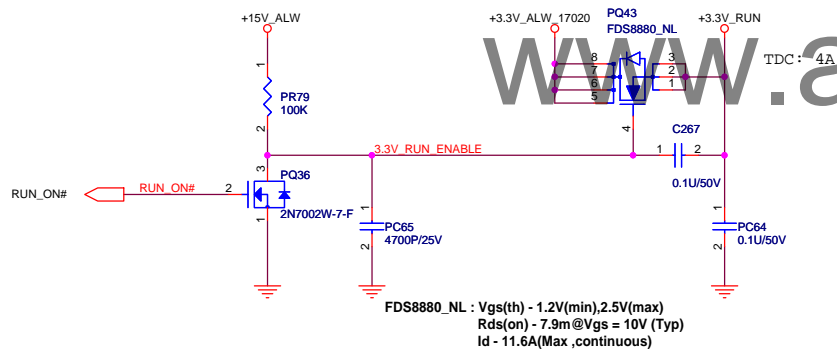
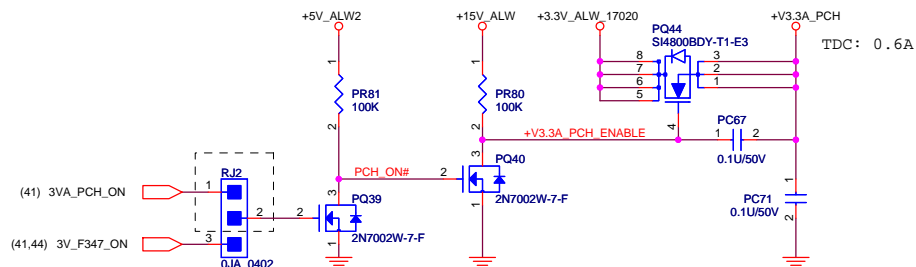
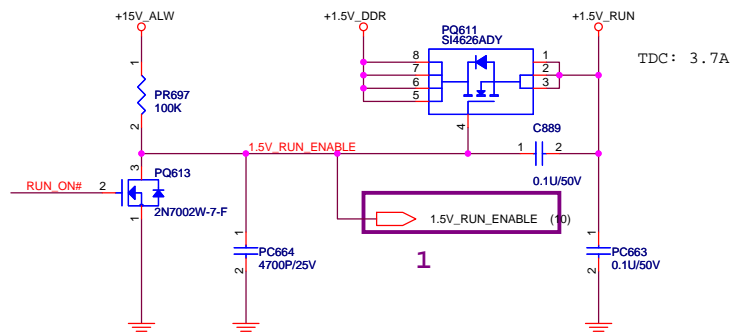


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Title		
+V1.8 (RT9025-25PSP)		
Size	Document Number	Rev
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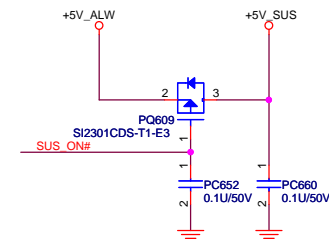
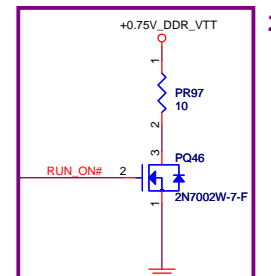
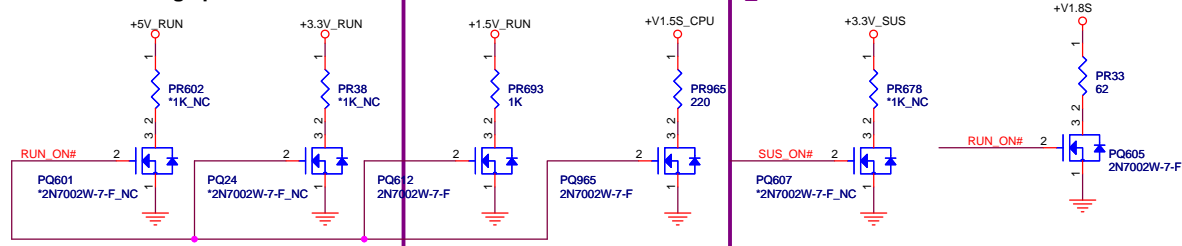


SI4336DY-T1-E3 :
Vgs(th) - 1.0V(min), 3.0V(max)
Rds(on) - 2.6m@Vgs = 10V (Typ)
Id - 17A(Max ,continuous)

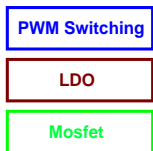
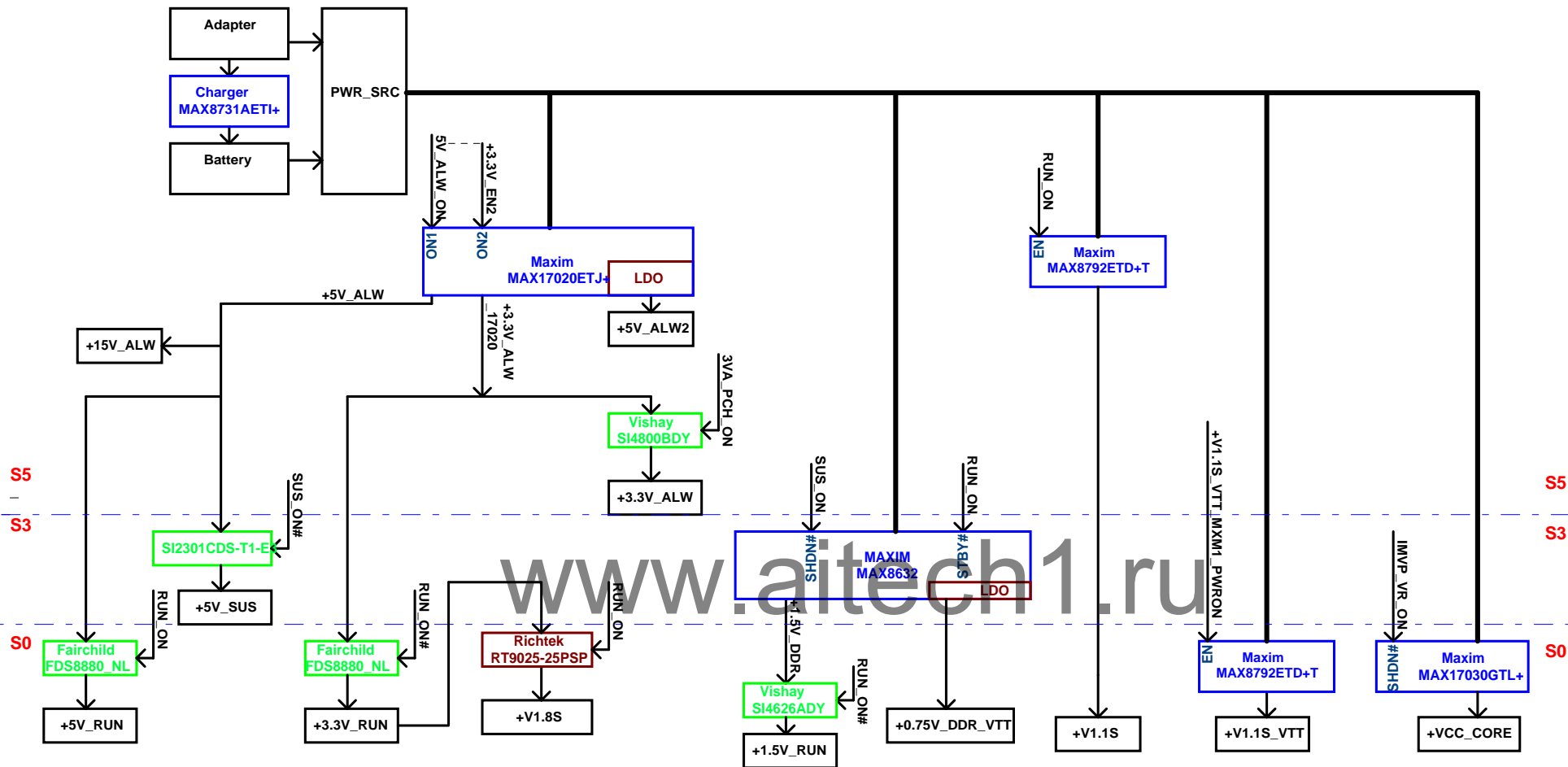


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Reserve discharge path



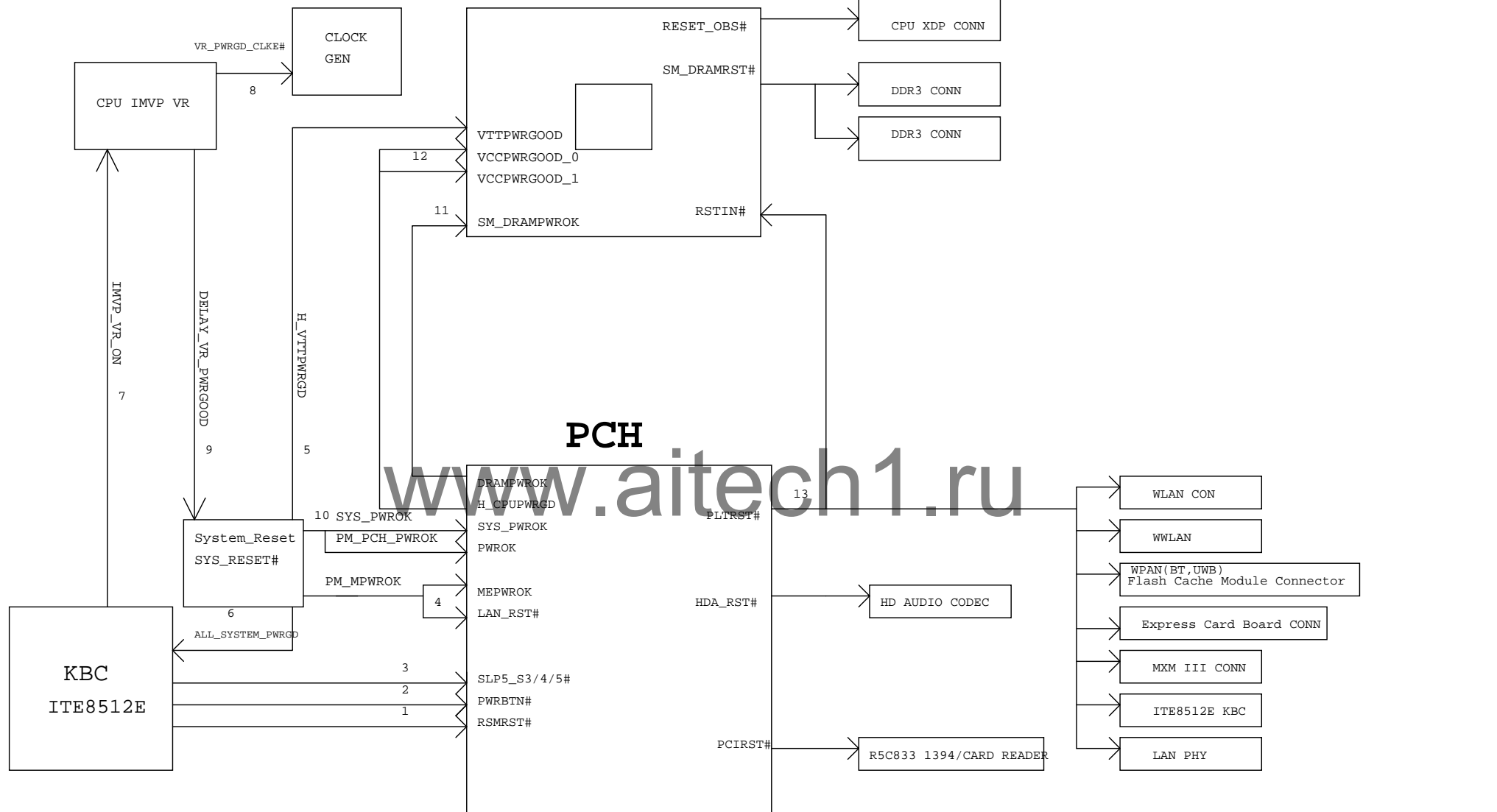
Title		
RUN POWER SW		
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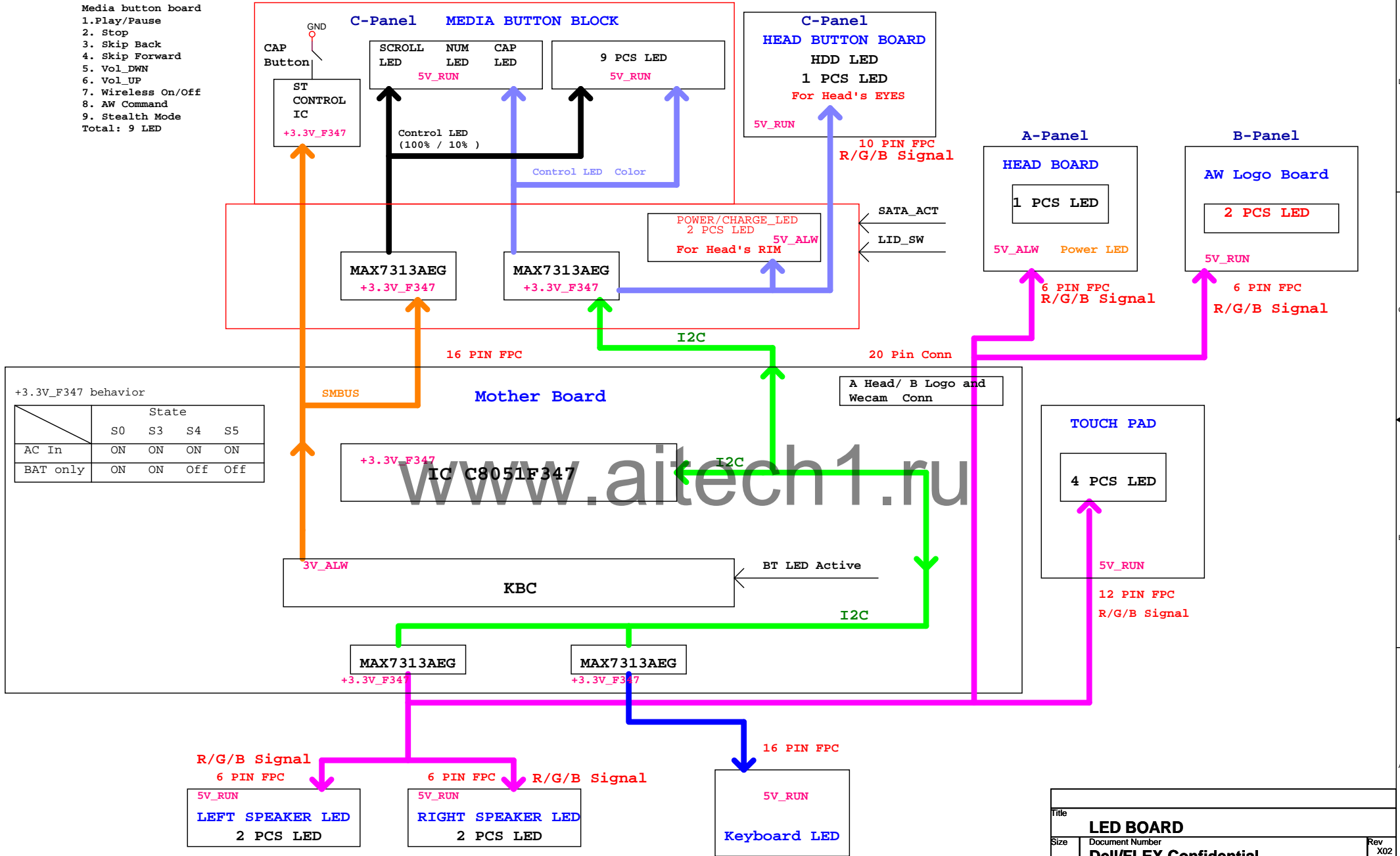
RESET MAP

CPU

PCH

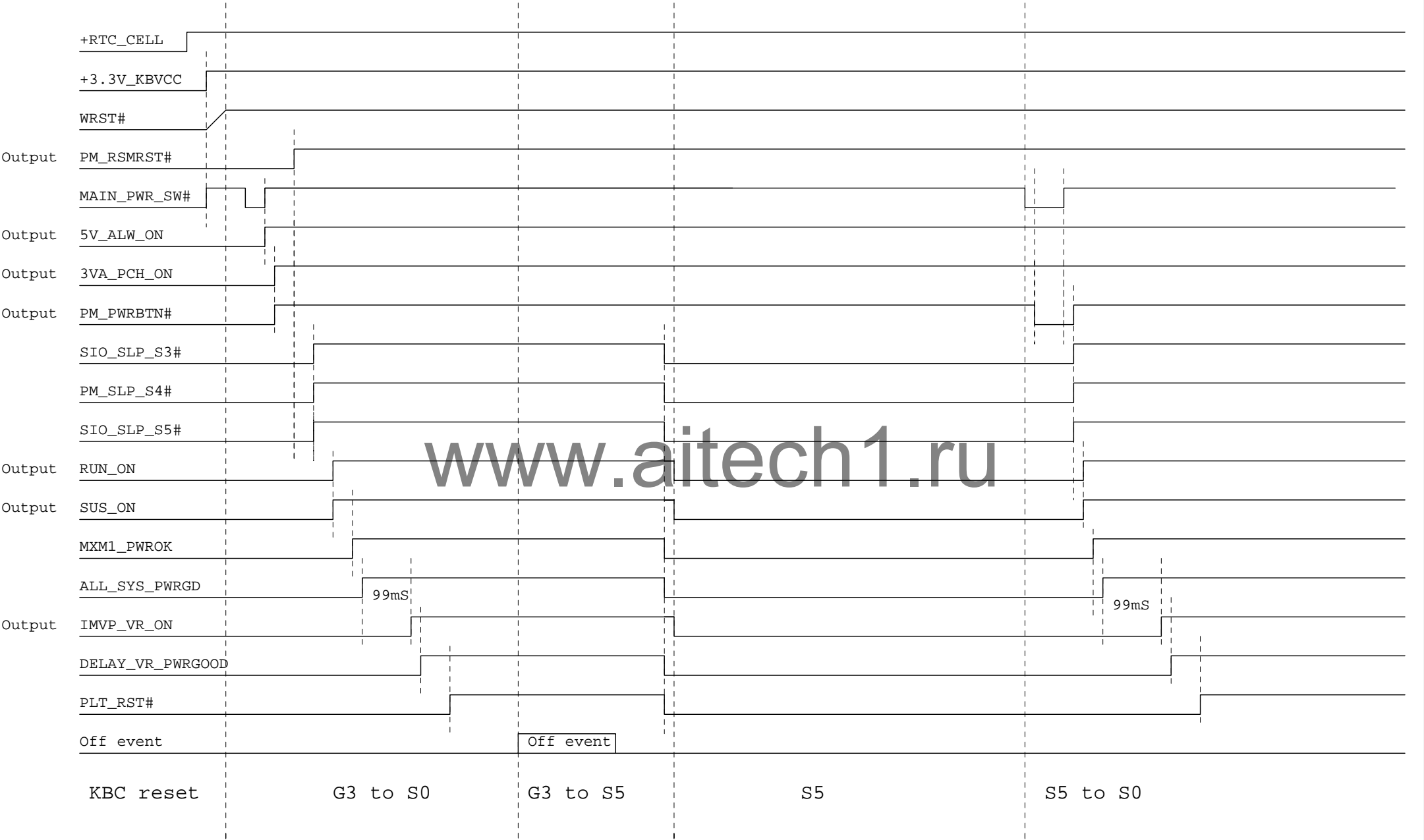


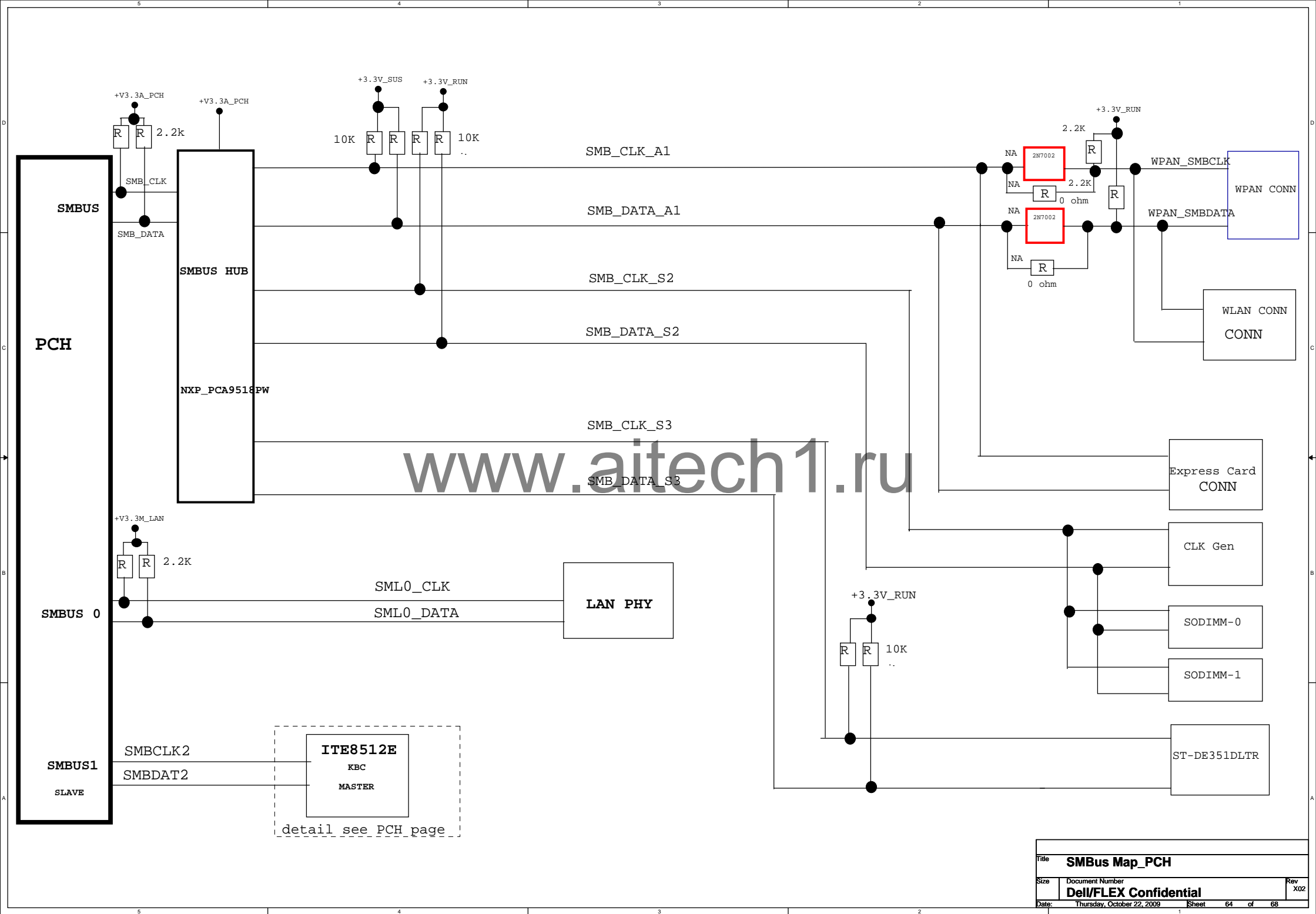
- Media button board
1. Play/Pause
 2. Stop
 3. Skip Back
 4. Skip Forward
 5. Vol_DWN
 6. Vol_UP
 7. Wireless On/Off
 8. AW Command
 9. Stealth Mode
- Total: 9 LED

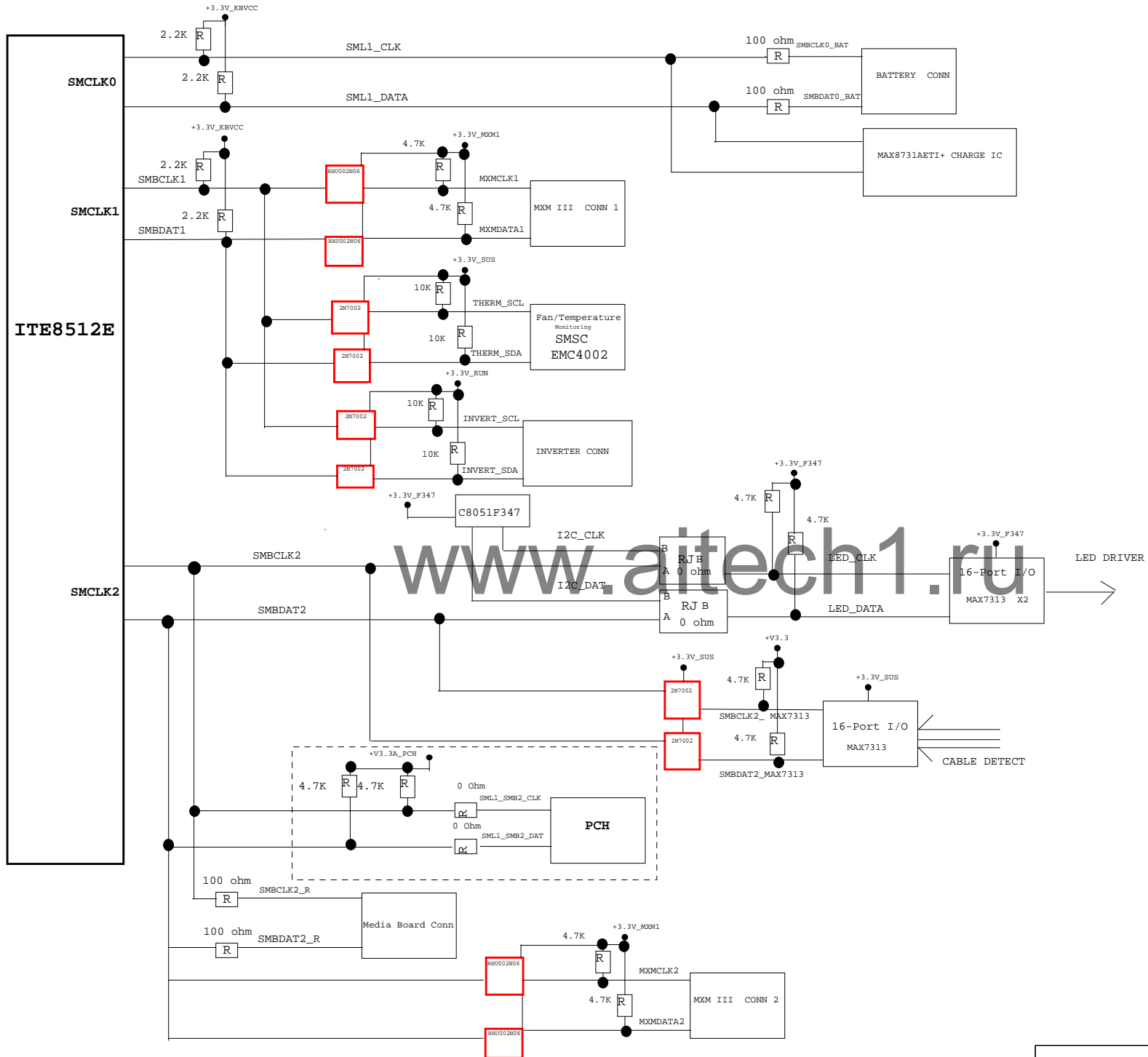


Title		
LED BOARD		
Size	Document Number	Rev
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KBC Powre Up Sequence







2009/02/18
1. Add power solution, power link() modify power name +V58 ->+5V_RUN, +V1.58->+1.5V_RUN, +V3.38->+3.3V_RUN, +V3.3->+3.3V_SBS, +V5->+5V_SBS...etc form CPU and Ibox)
2. P.45 Add ONFI connector
3. P.48 Change LAN to RAKEVILLE(R2577)
4. P.1 Modify function block
2009/02/23
1. change EC connect
2. Link USB line
3. Change PCI_GNT#0 to PCI_GNT#8
4. P.24 NVRAM power add a optional 1.8V sch, if ONFI used, using 1.8V
2009/02/24
1. change USB charger component
2. Add some GPIO of PCH for Hybrid
3. modify function block
2009/02/25
1. remove 2 DIMM
2. add EDP connector
3. remove P.50 original power sequence of QS and modify power sequence P.63 than copy to P.50
4. modify LAN chip link p.48
2009/02/26
1. modify the power link from LAN chip to transform and RJ45
2. modify some GPIO pin of P.68
2009/03/04
1. remove HYBRID switchable graphical card schematics
2. remove VGA power of processor and FDI bus for delete UGA support
2009/03/05
1. change SIM slot to WUMAX connector
2009/03/06
1. add PCI-E switch schematics
2009/03/10
1. modify MDM and system power sequence
2. add PM_SLP_S5 RLC to U42
3. p.3, p.4 description
2009/03/13
1. modify USB nets name from MCH to PCH
2. modify 3904 LIB of P.40
3. add MDM1_PWBOK and MDM2_PWBOK pull high
2009/03/16
1. modify power for placement
2009/03/17
1. modify p. 37, HDD, ODD power controller sch
2. modify MDM_PRESENT to fit Defiant design
3. change to eDP connector to 4 channel
2009/03/19
1. modify p. 23 GPIO
2. modify RPD schematics of MEMI
3. modify p. 55 3.3V power schematics
4. modify p. 56 2.5V feedback resistor
5. add 1.8V dis-charged
2009/03/20
1. modify power p. 51 and p. 57
2. add a reserve pull high resistor at MDM_THRO
3. complete PCI-E switch schematics
2009/03/23
1. delete P39, R383,R452 and P.38, R380,R416 for dual pull high.
2009/03/24
1. LAN_CLK_REQ#_N with two power source pull high, remove one
2. p. 19 SMBus HUB schematic modify, change mini PCI-E card to separte different power plan with the same channel, and add channel 3 pull high
3. move C1135, C1136, C1138 to p. 64
2009/03/26
1. add G-sensor at p. 37
2. combine +V1.18 and +V1.18_VTT with a power controller
3. add CPU core boost voltage function at p. 52
4. SMB1A2 and SMB1A2T2 with dual pull high resistor, remove one.
2009/03/30
1. Add jumper between MDM and power
2. remove +3.3V_MDM2 power and modify +3.3V_MDM2 to +3.3V_MDM1
3. CLK_PCH_SRC1_N from AK47 of IBOX was wrong, change to CLK_PCH_SRC2_P
4. MDM master, DE_HPD_SINK signal remove AND-gate
5. modify MDM1_PRESENT# schematic from MDM connector, original with logical gate to ZN7002
2009/04/02
1. remove mini card 3 and SIM card
2. change PUV power plan from run to sus
3. delete p. 40 all most stich cap.
4. integrate TTL logical to reduce the quantity
5. modify +3.3V_ALN to connect to +V3.3A_PCH
2009/06/16
1. modify the schematics to MSD V.3
2009/06/19
1. change the power controller in +V1.18 and +V1.18_VTT to MAX8792
2009/06/20
1. arrange the page number
2. modify the block diagram, frontpage and add smbus map and EBC power up sequence
3. modify the SMBus of Winax and BT connector as Defiant
2009/06/22
1. modify express card connector definition to differentiate the QS. MLK express card daughter board need to modify. In order to avoid the QS DB enter MLK or MLK DB enter QS, change the pin definition to cut the card reader power.
2. separte MDM2 power
3. change IR power plane to +3.3V_ALM_17020 because of +V3.3A_PCH will be cut when shut down in battery .mode
4. remove TPM and thermal IC un-used part
5. modify U6.18 pin VDD_PWBMD Design
6. add second SATA HDD redriver IC
2009/06/30
1. P51 AGNDC net was not connect to system GND, change AGNDC to GND
2. P39 change PCI-E latch connector to SCREW part
3. change U21 pin UDI00 to PCI-E clock request
2009/07/02
1. change U17 part because Capella do not need combine the BIOS into EC flash
2. correct power PDE05 schematics
2009/07/06
1. Add EMI stitching CAP
2009/07/08
1. Add CRT DUAL PI filter and by-pass CAP for EMI
2009/07/09
1. reserve IC0PLAS1185 co-layout schematics for over-clock function
2. change MDM output configuration to below

MLK Define	For NV			For AMD	
	N10E-GTX1	N11E-GTX1	N11E-GS1/GE1	M98	Broadway
DPA	HDMI *	HDMI	HDMI	HDMI	HDMI
DPB	No Function	No Function	No Function	No Function	No Function
DPC	No Function	DP *	DP	DP	DP
DPD	No Function	eDP *	eDP	No Function	eDP

2009/07/13
1. modify HDM1_TX*_N and HDM1_TX*_P
2009/07/13
1. rename

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HISTORY		
Document History		
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Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/08/4	S3 power reduce	S3 power reduce	X01	7, 10, 12, 21, 49, 54, 58	Intel cut off the +V1.5S_CPU power of CPU during S3, therefor , PM_DRAM_PWRGD_R and CPUDRAMRST# need to modify to controller by EC. Follow CRB's suggestion, the controller also need to reserve one from GPIO46 of PCH, original VRDD_1 need to change to GPIO15
2	HDD pin11	add spin-up delay schematic	X01	37	Using FFS_INT2_R of U7 signal to delay HDD spin-up
3 2009/08/5	S3 power reduce	S3 power reduce	X01	12, 41	find GPE1 of EC was not used, take the pin for S3 power reduce item controller
4 2009/08/10	S3 power reduce	Intel's review	X01	58	PR965 change to 220 ohm
5	HDD pin11	reserve the INT2 to PCH	X01	21, 37	add U7 int2 line to PCH's GPIO0 on P37 and P21
6	S3 power reduce	Intel's review	X01	14, 15	RJ6 and RJ8 change to mounted B
7	over voltage of VCore	wrong schematics	X01	51	modify PU601.2 connect to PU601.1 directly
8	HDD pin11	wrong schematics	X01	37	modify Q953 and Q954 with wrong direction
9 2009/08/12	ELC controller	LED light on S4	X01	44	add RJ950 for S4 to ELC controller
10	ONFI funtion remove	ONFI was not support	X01	22, 35	un-mounted J3, C448, R857, mounted R858
11	web cam power controller	reserve 7313 20pin	X01	41, 44	CAM_PWR_ON# change to output from U605
12	remove un-used EMI cap	remove un-used EMI cap	X01	48	remove C407, R413, C422, C424, C350, C426, R378
13	VCore overvoltage	X00 stage was not mounted	X01	51	Mounted PU601, PQ603, PQ604, PR606, PR620, PR612, PR618, PC608
14	Intel design guide	change the Cap with low ESR	X01	53	Change the PN of PC34, PC36
15	Power	High side Vds fail	X01	54	Mounted PR141, PC130
16	Power	Change Net to +5V_ALWP to enable SECFB	X01	55	Change the +5V_ALWP connect to PR52.2
17 2009/08/18	Power	Power fine tune and over voltage schematic's bom change	X01	51, 50,	Change PR679 value to 8.2k, change PR612, PR618 value to 309, mounted PR619, un-mounted PR621
18 2009/08/19	HDD pin11	change INT_2 connect	X01	21	change to GPIO48 of PCH connect to INT_2 of G-sensor
19	MXM2 power control	change the control signal from PCH to EC	X01	21, 41	MXM2_PRESENT#, MXM2_PWR_EN, MXM2_PWROK move to EC, add R973, R971, remove R799, R841
20 2009/08/20	Power	XMP over-voltage solution	X01	54	mounted PR127, Q54, PR129, PR125, Q56, PR134
21	EMI	change the by-pass resistor to choke of USB11	X01	31	un-mounted R43, R42, mounted L4
22	Power	to follow Clarksfield XE load line spec	X01	51	change PR607 to 5.23K
23	BID change to current value	change BID to PT stage	X01	21	mounted R720, un-mounted R721
24	LAN EA fail issue	modify the layout for LAN routing	X01	48	Swap the pin assign of L34, L33 for routing
25	EMI	change the by-pass resistor to choke of USB2	X01	36	un-mounted R433, R434, mounted L38
26 2009/08/22	EMI	Modify RC priority of Media card interface	X01	46	Media card interface from U13 to CN15, original a Cap decoupling then damping a serious resistor change to damping a serious first, then a Cap add.
27 2009/08/25	remove ONFI	remove ONFI	X01	20	un-mounted R284
28	remove EEPROM of media card/1394	change to BIOS confige the controller	X01	46	un-mounted U10, R241. mounted R229
29 2009/08/26	Power	150W power support	X01	50	change PR138 to 10.7k for 150W power support
30	Slave VGA leakage issue	add power split component	X01	27	1. solve RST signal leakage: add a AND gate and R977, R976. 2. ACAV_IN signal leakage: sepearate MXM1 and MXM2, add Q956, R975, Q957 3. CLKREQ signal leakage: add Q958 to cut clkreq if MXM2 power disable. 4. combine THERM_MXM1#, THERM_MXM2# to THERM_MXM#, change GPA5 of EC(original THERM_MXM1#) to MXM_RST.
31 2009/08/27	EMI	add decoupling CAP for EMI	X01	59	+3.3V_RUN add C956, C957, C958, C959, +5V_ALW add C963, C960, C962, C961
32	power leakage	+5V_SUS leakage, change power source of PU6	X01	54	modify PR100 connect to +5V_ALW
33	power leakage	+V3.3M_LAN leakage	X01	47	add R981, R980, Q959 to split two power plane
34	power leakage	+3.3V_SUS leakage	X01	41	un-mount R113

Item	Fix Issue	Reason to change	Rev	Page	Modify list
1 2009/09/30	KB LED light uneven	different resistor value of the pin	X02	44	change R748 to 0ohm
2	VCore power	for second source used	X02	51	Change to mount PC16, PC17, PC622, PC19, PC14, PC13, PR660, PR646, PC636, PC619 for second source
3	charger		X02	50	change PL7, and mounted PR102, PC90
4	modify OCP	modify +V1.1S OCP value	X02	52	change PR88 value
5	3V/5V power	for second source used	X02	55	mounted PR76, PC54, PR75, PC57, change PR41, PR65 value
6	SI measure	add EMI solution will cause SI fail	X02	36	un-mounted L38 and mounted R433, R434
7 2009/10/2	over clock	change over-clock clock GEN	X02	5	change U3 to ICS3185, mounted L16, C139, un-mounted R88, R114
8	remove HDD2 redriver IC	SI could pass without re-driver IC	X02	37	remove C52, C51, C69, C68, U2, C54, C58, C61, C62, R50, R51, R52, R53, R54
9 2009/10/19	tuning the RTC timing	RTC timing will fail in some system in setup menu	X02	16	change C243 to 15pF
10	FDIM test fix	FDIM test fix	X02	9	change C768, C764, C650, C765, C766, C756, C186, C187, C192, C149, C150, C151, C152, C153, C154, C155 to 22uF, change PR634 to 255k ohm, change PC618, PC627, PC616 to 0.22uF/16V, Change PC623, PC617, and PC632 to mount, Change PC635, PC626, PC630, PC631, PC629, PC628 to 470uF/ESR4.5mohm.
11 2009/10/21	MXM2 power leakage	+3.3V_MXM2 with power leakage	X02	27, 28	add D953, D954, D955
12 2009/11/24	LAN LED	LAN LED will light if un-plug LAN and disable LAN function	A00	48	CN19.B1 change to connect to power, and CN19.B2 change to connect to R405.1

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